

# MSP430C11x1, MSP430F11x1A MIXED SIGNAL MICROCONTROLLER

SLAS241H – SEPTEMBER 1999 – REVISED SEPTEMBER 2004

- Low Supply Voltage Range 1.8 V to 3.6 V
- Ultralow-Power Consumption
  - Active Mode: 160  $\mu$ A at 1 MHz, 2.2 V
  - Standby Mode: 0.7  $\mu$ A
  - Off Mode (RAM Retention): 0.1  $\mu$ A
- Wake-Up From Standby Mode in less than 6  $\mu$ s
- 16-Bit RISC Architecture, 125 ns Instruction Cycle Time
- Basic Clock Module Configurations:
  - Various Internal Resistors
  - Single External Resistor
  - 32-kHz Crystal
  - High-Frequency Crystal
  - Resonator
  - External Clock Source
- 16-Bit Timer\_A With Three Capture/Compare Registers
- On-Chip Comparator for Analog Signal Compare Function or Slope A/D Conversion
- Serial Onboard Programming, No External Programming Voltage Needed Programmable Code Protection by Security Fuse
- Family Members Include:
  - MSP430C1101: 1KB ROM, 128B RAM
  - MSP430C1111: 2KB ROM, 128B RAM
  - MSP430C1121: 4KB ROM, 256B RAM
  - MSP430F1101A: 1KB + 128B Flash Memory 128B RAM
  - MSP430F1111A: 2KB + 256B Flash Memory 128B RAM
  - MSP430F1121A: 4KB + 256B Flash Memory 256B RAM
- Available in a 20-Pin Plastic Small-Outline Wide Body (SOWB) Package, 20-Pin Plastic Small-Outline Thin Package, 20-Pin TVSOP (F11x1A only) and 24-Pin QFN
- For Complete Module Descriptions, Refer to the *MSP430x1xx Family User's Guide*, Literature Number SLAU049

## description

The Texas Instruments MSP430 family of ultralow power microcontrollers consist of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low power modes is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that attribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 6 $\mu$ s. The MSP430x11x1(A) series is an ultralow-power mixed signal microcontroller with a built-in 16-bit timer, versatile analog comparator and fourteen I/O pins.

Typical applications include sensor systems that capture analog signals, convert them to digital values, and then process the data for display or for transmission to a host system. Stand alone RF sensor front end is another area of application. The I/O port inputs provide single slope A/D conversion capability on resistive sensors.

### AVAILABLE OPTIONS

| TA            | PACKAGED DEVICES  |   |  |   |
|---------------|---|---|--|---|
|               | PLASTIC 20-PIN SOWB (DW)  | PLASTIC 20-PIN TSSOP (PW)   | PLASTIC 20-PIN TVSOP (DGV)                               | PLASTIC 24-PIN QFN (RGE)  |
| -40°C to 85°C | MSP430C1101IDW<br>MSP430C1111IDW<br>MSP430C1121IDW<br>MSP430F1101AIDW<br>MSP430F1111AIDW<br>MSP430F1121AIDW | MSP430C1101IPW<br>MSP430C1111IPW<br>MSP430C1121IPW<br>MSP430F1101AIPW<br>MSP430F1111AIPW<br>MSP430F1121AIPW | MSP430F1101AIDGV<br>MSP430F1111AIDGV<br>MSP430F1121AIDGV | MSP430C1101IRGE<br>MSP430C1111IRGE<br>MSP430C1121IRGE<br>MSP430F1101AIRGE<br>MSP430F1111AIRGE<br>MSP430F1121AIRGE |



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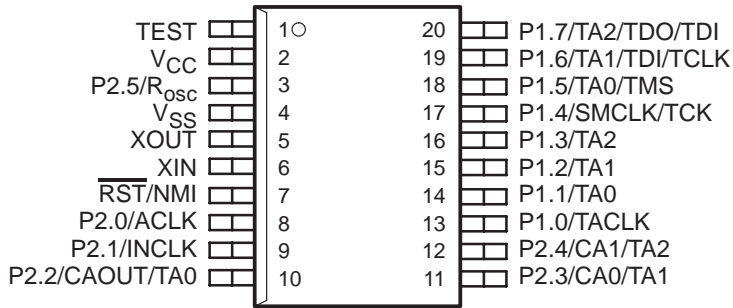
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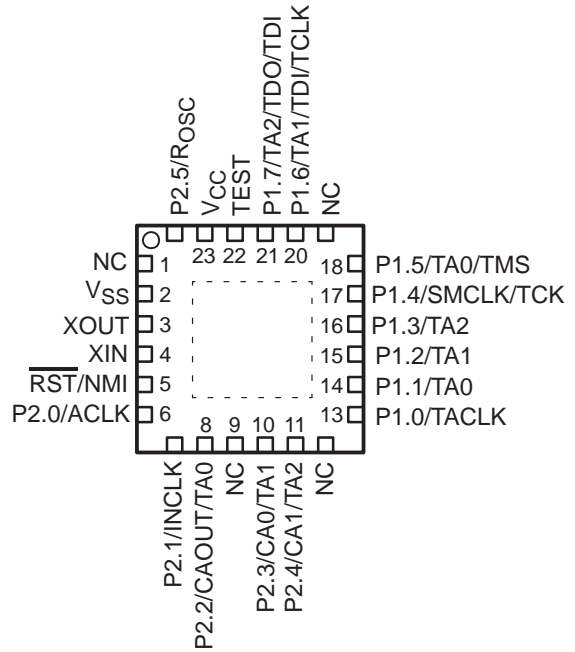
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DW, PW, or DGV PACKAGE  
(TOP VIEW)

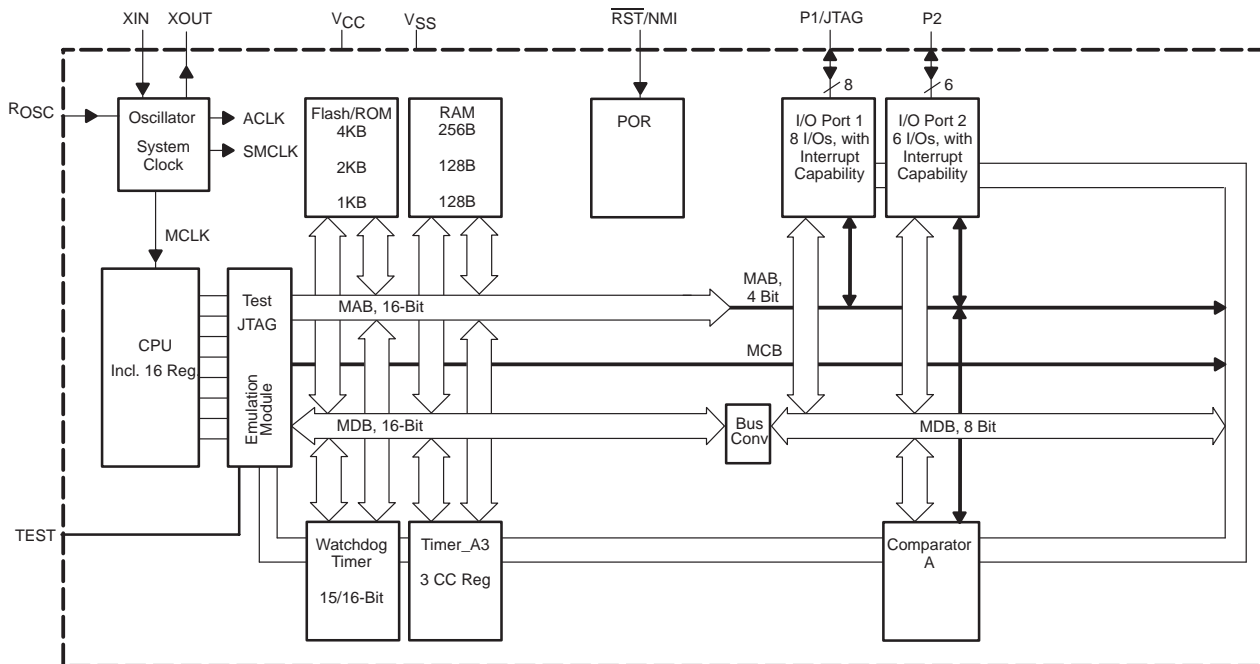


RGE PACKAGE  
(TOP VIEW)



Note: NC pins not internally connected  
Power Pad connection to V<sub>SS</sub> recommended

## functional block diagram



# MSP430C11x1, MSP430F11x1A MIXED SIGNAL MICROCONTROLLER

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## Terminal Functions

| TERMINAL          |                    |             |     | DESCRIPTION  |
|-------------------|--------------------|-------------|-----|--|
| NAME              | DW, PW, or DGV NO. | RGE NO.     | I/O |  |
| P1.0/TACLK        | 13                 | 13          | I/O | General-purpose digital I/O pin/Timer_A, clock signal TACLK input  |
| P1.1/TA0          | 14                 | 14          | I/O | General-purpose digital I/O pin/Timer_A, capture: CC10A input, compare: Out0 output/BSL transmit                               |
| P1.2/TA1          | 15                 | 15          | I/O | General-purpose digital I/O pin/Timer_A, capture: CC11A input, compare: Out1 output  |
| P1.3/TA2          | 16                 | 16          | I/O | General-purpose digital I/O pin/Timer_A, capture: CC12A input, compare: Out2 output  |
| P1.4/SMCLK/TCK    | 17                 | 17          | I/O | General-purpose digital I/O pin/SMCLK signal output/test clock, input terminal for device programming and test                 |
| P1.5/TA0/TMS      | 18                 | 18          | I/O | General-purpose digital I/O pin/Timer_A, compare: Out0 output/test mode select, input terminal for device programming and test |
| P1.6/TA1/TDI/TCLK | 19                 | 20          | I/O | General-purpose digital I/O pin/Timer_A, compare: Out1 output/test data input or test clock input                              |
| P1.7/TA2/TDO/TDI† | 20                 | 21          | I/O | General-purpose digital I/O pin/Timer_A, compare: Out2 output/test data output terminal or data input during programming       |
| P2.0/ACLK         | 8                  | 6           | I/O | General-purpose digital I/O pin/ACLK output  |
| P2.1/INCLK        | 9                  | 7           | I/O | General-purpose digital I/O pin/Timer_A, clock signal at INCLK   |
| P2.2/CAOUT/TA0    | 10                 | 8           | I/O | General-purpose digital I/O pin/Timer_A, capture: CC10B input/comparator_A, output/BSL receive                                 |
| P2.3/CA0/TA1      | 11                 | 10          | I/O | General-purpose digital I/O pin/Timer_A, compare: Out1 output/comparator_A, input  |
| P2.4/CA1/TA2      | 12                 | 11          | I/O | General-purpose digital I/O pin/Timer_A, compare: Out2 output/comparator_A, input  |
| P2.5/ROSC         | 3                  | 24          | I/O | General-purpose digital I/O pin/input for external resistor that defines the DCO nominal frequency                             |
| RST/NMI           | 7                  | 5           | I   | Reset or nonmaskable interrupt input   |
| TEST              | 1                  | 22          | I   | Selects test mode for JTAG pins on Port1. The device protection fuse is connected to TEST.                                     |
| VCC               | 2                  | 23          |     | Supply voltage   |
| VSS               | 4                  | 2           |     | Ground reference   |
| XIN               | 6                  | 4           | I   | Input terminal of crystal oscillator   |
| XOUT              | 5                  | 3           | O   | Output terminal of crystal oscillator  |
| QFN Pad           | NA                 | Package Pad | NA  | QFN package pad connection to VSS recommended.   |

† TDO or TDI is selected via JTAG instruction.



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## short-form description

### CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

### instruction set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 1 shows examples of the three types of instruction formats; the address modes are listed in Table 2.

|                          |           |
|--------------------------|-----------|
| Program Counter          | PC/R0     |
| Stack Pointer            | SP/R1     |
| Status Register          | SR/CG1/R2 |
| Constant Generator       | CG2/R3    |
| General-Purpose Register | R4        |
| General-Purpose Register | R5        |
| General-Purpose Register | R6        |
| General-Purpose Register | R7        |
| General-Purpose Register | R8        |
| General-Purpose Register | R9        |
| General-Purpose Register | R10       |
| General-Purpose Register | R11       |
| General-Purpose Register | R12       |
| General-Purpose Register | R13       |
| General-Purpose Register | R14       |
| General-Purpose Register | R15       |

**Table 1. Instruction Word Formats**

|                                   |                |                       |
|-----------------------------------|----------------|-----------------------|
| Dual operands, source-destination | e.g. ADD R4,R5 | R4 + R5 ----> R5      |
| Single operands, destination only | e.g. CALL R8   | PC -->(TOS), R8--> PC |
| Relative jump, un/conditional     | e.g. JNE       | Jump-on-equal bit = 0 |

**Table 2. Address Mode Descriptions**

| ADDRESS MODE           | S | D | SYNTAX          | EXAMPLE          | OPERATION                        |
|------------------------|---|---|-----------------|------------------|----------------------------------|
| Register               | ● | ● | MOV Rs,Rd       | MOV R10,R11      | R10 --> R11                      |
| Indexed                | ● | ● | MOV X(Rn),Y(Rm) | MOV 2(R5),6(R6)  | M(2+R5)--> M(6+R6)               |
| Symbolic (PC relative) | ● | ● | MOV EDE,TONI    |                  | M(EDE) --> M(TONI)               |
| Absolute               | ● | ● | MOV &MEM,&TCDAT |                  | M(MEM) --> M(TCDAT)              |
| Indirect               | ● |   | MOV @Rn,Y(Rm)   | MOV @R10,Tab(R6) | M(R10) --> M(Tab+R6)             |
| Indirect autoincrement | ● |   | MOV @Rn+,Rm     | MOV @R10+,R11    | M(R10) --> R11<br>R10 + 2--> R10 |
| Immediate              | ● |   | MOV #X,TONI     | MOV #45,TONI     | #45 --> M(TONI)                  |

NOTE: S = source D = destination



## operating modes

The MSP430 has one active mode and five software selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode AM;
  - All clocks are active
- Low-power mode 0 (LPM0);
  - CPU is disabled  
ACLK and SMCLK remain active. MCLK is disabled
- Low-power mode 1 (LPM1);
  - CPU is disabled  
ACLK and SMCLK remain active. MCLK is disabled  
DCO's dc-generator is disabled if DCO not used in active mode
- Low-power mode 2 (LPM2);
  - CPU is disabled  
MCLK and SMCLK are disabled  
DCO's dc-generator remains enabled  
ACLK remains active
- Low-power mode 3 (LPM3);
  - CPU is disabled  
MCLK and SMCLK are disabled  
DCO's dc-generator is disabled  
ACLK remains active
- Low-power mode 4 (LPM4);
  - CPU is disabled  
ACLK is disabled  
MCLK and SMCLK are disabled  
DCO's dc-generator is disabled  
Crystal oscillator is stopped

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## interrupt vector addresses

The interrupt vectors and the power-up starting address are located in the address range of 0FFFFh–0FFE0h. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

| INTERRUPT SOURCE   | INTERRUPT FLAG   | SYSTEM INTERRUPT                                     | WORD ADDRESS | PRIORITY    |
|--|--|--|--------------|-------------|
| Power-up<br>External reset<br>Watchdog<br>Flash Memory   | WDTIFG<br>KEYV<br>(see Note 1)                           | Reset  | 0FFFEh       | 15, highest |
| NMI<br>Oscillator fault<br>Flash memory access violation | NMIIFG<br>OFIFG<br>ACCVIFG<br>(see Notes 1 & 4)          | (non)-maskable,<br>(non)-maskable,<br>(non)-maskable | 0FFFCh       | 14          |
|  |  |  | 0FFFAh       | 13          |
|  |  |  | 0FFF8h       | 12          |
| Comparator_A   | CAIFG  | maskable   | 0FFF6h       | 11          |
| Watchdog Timer   | WDTIFG   | maskable   | 0FFF4h       | 10          |
| Timer_A3   | TACCR0 CCIFG (see Note 2)                                | maskable   | 0FFF2h       | 9           |
| Timer_A3   | TACCR1 CCIFG.<br>TACCR2 CCIFG<br>TAIFG (see Notes 1 & 2) | maskable   | 0FFF0h       | 8           |
|  |  |  | 0FEEh        | 7           |
|  |  |  | 0FEECh       | 6           |
|  |  |  | 0FEEAh       | 5           |
|  |  |  | 0FEE8h       | 4           |
| I/O Port P2<br>(eight flags; see Note 3)                 | P2IFG.0 to P2IFG.7<br>(see Notes 1 & 2)                  | maskable   | 0FEE6h       | 3           |
| I/O Port P1<br>(eight flags)                             | P1IFG.0 to P1IFG.7<br>(see Notes 1 & 2)                  | maskable   | 0FEE4h       | 2           |
|  |  |  | 0FEE2h       | 1           |
|  |  |  | 0FEE0h       | 0, lowest   |

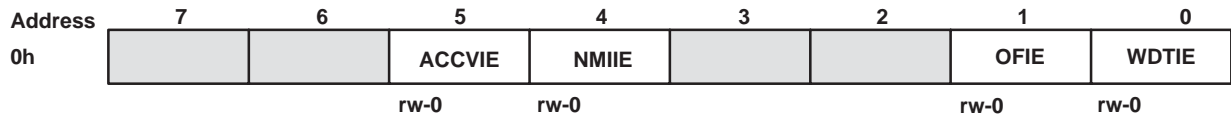
- NOTES:
- Multiple source flags
  - Interrupt flags are located in the module
  - There are eight Port P2 interrupt flags, but only six Port P2 I/O pins (P2.0–5) implemented on the 'C11x1 and 'F11x1A devices.
  - (non)-maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt enable cannot.  
Nonmaskable: neither the individual nor the general interrupt-enable bit will disable an interrupt event.



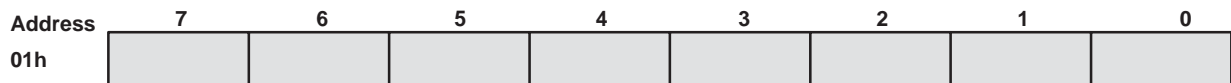
### special function registers

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.

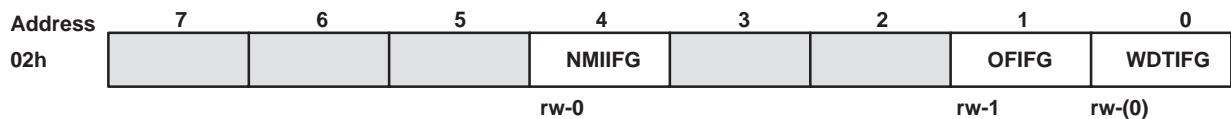
#### interrupt enable 1 and 2



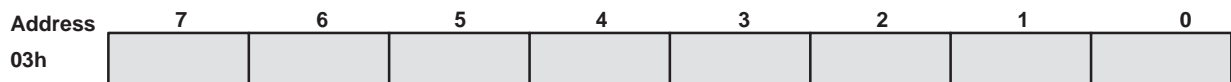
- WDTIE: Watchdog Timer interrupt enable. Inactive if watchdog mode is selected. Active if Watchdog Timer is configured in interval timer mode.
- OFIE: Oscillator fault enable
- NMIIE: (Non)maskable interrupt enable
- ACCVIE: Flash access violation interrupt enable



#### interrupt flag register 1 and 2



- WDTIFG: Set on Watchdog Timer overflow (in watchdog mode) or security key violation. Reset on  $V_{CC}$  power-up or a reset condition at RST/NMI pin in reset mode.
- OFIFG: Flag set on oscillator fault
- NMIIFG: Set via RST/NMI-pin



- Legend**
- rw:** Bit can be read and written.
- rw-0,1:** Bit can be read and written. It is Reset or Set by PUC.
- rw-(0,1):** Bit can be read and written. It is Reset or Set by POR.
- SFR bit is not present in device

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## memory organization

|   |                              | MSP430C1101                               | MSP430C1111                               | MSP430C1121                               |
|---|------------------------------|---|---|---|
| Memory<br>Main: interrupt vector<br>Main: code memory | Size<br>ROM                  | 1KB ROM<br>0FFFFh–0FFE0h<br>0FFFFh–0FC00h | 2KB ROM<br>0FFFFh–0FFE0h<br>0FFFFh–0F800h | 4KB ROM<br>0FFFFh–0FFE0h<br>0FFFFh–0F000h |
|   | Information memory           | Not applicable                            | Not applicable                            | Not applicable                            |
| Boot memory   | Size<br>ROM                  | Not applicable                            | Not applicable                            | Not applicable                            |
| RAM   | Size                         | 128 Byte<br>027Fh – 0200h                 | 128 Byte<br>027Fh – 0200h                 | 256 Byte<br>02FFh – 0200h                 |
| Peripherals   | 16-bit<br>8-bit<br>8-bit SFR | 01FFh – 0100h<br>0FFh – 010h<br>0Fh – 00h | 01FFh – 0100h<br>0FFh – 010h<br>0Fh – 00h | 01FFh – 0100h<br>0FFh – 010h<br>0Fh – 00h |

|   |                              | MSP430F1101A                                | MSP430F1111A                                | MSP430F1121A                                |
|---|------------------------------|---|---|---|
| Memory<br>Main: interrupt vector<br>Main: code memory | Size<br>Flash                | 1KB Flash<br>0FFFFh–0FFE0h<br>0FFFFh–0FC00h | 2KB Flash<br>0FFFFh–0FFE0h<br>0FFFFh–0F800h | 4KB Flash<br>0FFFFh–0FFE0h<br>0FFFFh–0F000h |
|   | Information memory           | Size<br>Flash                               | 128 Byte<br>010FFh – 01080h                 | 256 Byte<br>010FFh – 01000h                 |
| Boot memory   | Size<br>ROM                  | 1KB<br>0FFFh – 0C00h                        | 1KB<br>0FFFh – 0C00h                        | 1KB<br>0FFFh – 0C00h                        |
| RAM   | Size                         | 128 Byte<br>027Fh – 0200h                   | 128 Byte<br>027Fh – 0200h                   | 256 Byte<br>02FFh – 0200h                   |
| Peripherals   | 16-bit<br>8-bit<br>8-bit SFR | 01FFh – 0100h<br>0FFh – 010h<br>0Fh – 00h   | 01FFh – 0100h<br>0FFh – 010h<br>0Fh – 00h   | 01FFh – 0100h<br>0FFh – 010h<br>0Fh – 00h   |

## bootstrap loader (BSL)

The MSP430 bootstrap loader (BSL) enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by user-defined password. For complete description of the features of the BSL and its implementation, see the Application report *Features of the MSP430 Bootstrap Loader*, Literature Number SLAA089.

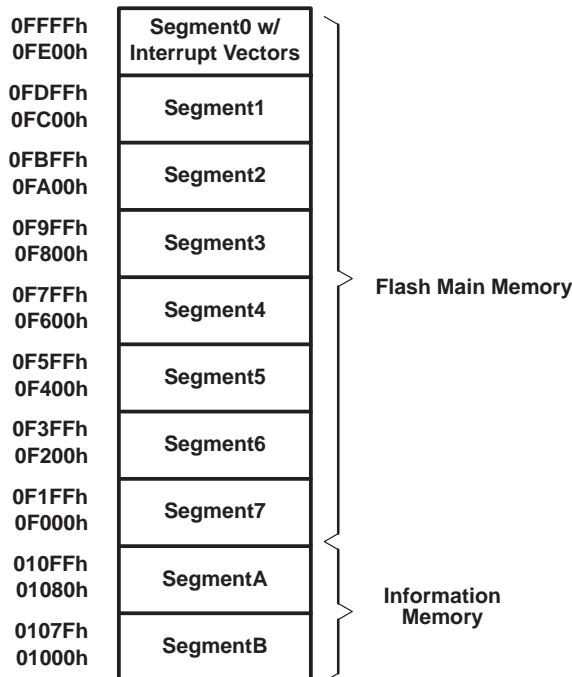
| BSL Function  | DW, PW & DGV Package Pins | RGE Package Pins |
|---------------|---------------------------|------------------|
| Data Transmit | 14 - P1.1                 | 14 - P1.1        |
| Data Receive  | 10 - P2.2                 | 8 - P2.2         |



**flash memory**

The flash memory can be programmed via the JTAG port, the bootstrap loader, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and two segments of information memory (A and B) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A and B can be erased individually, or as a group with segments 0–n. Segments A and B are also called *information memory*.
- New devices may have some bytes programmed in the information memory (needed for test during manufacturing). The user should perform an erase of the information memory prior to the first use.



NOTE: All segments not implemented on all devices.

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## peripherals

Peripherals are connected to the CPU through data, address, and control busses and can be handled using all instructions. For complete module descriptions, refer to the *MSP430x1xx Family User's Guide*, literature number SLAU049.

## oscillator and system clock

The clock system is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal digitally-controlled oscillator (DCO) and a high frequency crystal oscillator. The basic clock module is designed to meet the requirements of both low system cost and low-power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 6  $\mu$ s. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal or a high frequency crystal.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules.

## digital I/O

There are two 8-bit I/O ports implemented—ports P1 and P2 (only six P2 I/O signals are available on external pins):

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Edge-selectable interrupt input capability for all the eight bits of port P1 and six bits of port P2.
- Read/write access to port-control registers is supported by all instructions.

### NOTE:

Six bits of port P2, P2.0 to P2.5, are available on external pins – but all control and data bits for port P2 are implemented.

## watchdog timer

The primary function of the watchdog timer (WDT) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

## comparator\_A

The primary function of the comparator\_A module is to support precision slope analog-to-digital conversions, battery-voltage supervision, and monitoring of external analog signals.

**timer\_A3**

Timer\_A3 is a 16-bit timer/counter with three capture/compare registers. Timer\_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer\_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

| Timer_A3 Signal Connections |           |                     |                   |              |                      |                   |           |
|-----------------------------|-----------|---------------------|-------------------|--------------|----------------------|-------------------|-----------|
| Input Pin Number            |           | Device Input Signal | Module Input Name | Module Block | Module Output Signal | Output Pin Number |           |
| DW, PW, DGV                 | RGE       |                     |                   |              |                      | DW, PW DGV        | RGE       |
| 13 - P1.0                   | 13 - P1.0 | TACLK               | TACLK             | Timer        | NA                   |                   |           |
|                             |           | ACLK                | ACLK              |              |                      |                   |           |
|                             |           | SMCLK               | SMCLK             |              |                      |                   |           |
| 9 - P2.1                    | 7 - P2.1  | INCLK               | INCLK             |              |                      |                   |           |
| 14 - P1.1                   | 14 - P1.1 | TA0                 | CCI0A             | CCR0         | TA0                  | 14 - P1.1         | 14 - P1.1 |
| 10 - P2.2                   | 8 - P2.2  | TA0                 | CCI0B             |              |                      | 18 - P1.5         | 18 - P1.5 |
|                             |           | VSS                 | GND               |              |                      |                   |           |
|                             |           | VCC                 | VCC               |              |                      |                   |           |
| 15 - P1.2                   | 15 - P1.2 | TA1                 | CCI1A             | CCR1         | TA1                  | 11 - P2.3         | 10 - P2.3 |
|                             |           | CAOUT (internal)    | CCI1B             |              |                      | 15 - P1.2         | 15 - P1.2 |
|                             |           | VSS                 | GND               |              |                      | 19 - P1.6         | 20 - P1.6 |
|                             |           | VCC                 | VCC               |              |                      |                   |           |
| 16 - P1.3                   | 16 - P1.3 | TA2                 | CCI2A             | CCR2         | TA2                  | 12 - P2.4         | 11 - P2.4 |
|                             |           | ACLK (internal)     | CCI2B             |              |                      | 16 - P1.3         | 16 - P1.3 |
|                             |           | VSS                 | GND               |              |                      | 20 - P1.7         | 21 - P1.7 |
|                             |           | VCC                 | VCC               |              |                      |                   |           |

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## peripheral file map

| PERIPHERALS WITH WORD ACCESS |                               |         |       |
|------------------------------|-------------------------------|---------|-------|
| <b>Timer_A</b>               | Reserved                      |         | 017Eh |
|                              | Reserved                      |         | 017Ch |
|                              | Reserved                      |         | 017Ah |
|                              | Reserved                      |         | 0178h |
|                              | Capture/compare register      | TACCR2  | 0176h |
|                              | Capture/compare register      | TACCR1  | 0174h |
|                              | Capture/compare register      | TACCR0  | 0172h |
|                              | Timer_A register              | TAR     | 0170h |
|                              | Reserved                      |         | 016Eh |
|                              | Reserved                      |         | 016Ch |
|                              | Reserved                      |         | 016Ah |
|                              | Reserved                      |         | 0168h |
|                              | Capture/compare control       | TACCTL2 | 0166h |
|                              | Capture/compare control       | TACCTL1 | 0164h |
| Capture/compare control      | TACCTL0                       | 0162h   |       |
| Timer_A control              | TACTL                         | 0160h   |       |
| Timer_A interrupt vector     | TAIV                          | 012Eh   |       |
| <b>Flash Memory</b>          | Flash control 3               | FCTL3   | 012Ch |
|                              | Flash control 2               | FCTL2   | 012Ah |
|                              | Flash control 1               | FCTL1   | 0128h |
| <b>Watchdog</b>              | Watchdog/timer control        | WDTCTL  | 0120h |
| PERIPHERALS WITH BYTE ACCESS |                               |         |       |
| <b>Comparator_A</b>          | Comparator_A port disable     | CAPD    | 05Bh  |
|                              | Comparator_A control 2        | CACTL2  | 05Ah  |
|                              | Comparator_A control 1        | CACTL1  | 059h  |
| <b>Basic Clock</b>           | Basic clock system control 2  | BCSCTL2 | 058h  |
|                              | Basic clock system control 1  | BCSCTL1 | 057h  |
|                              | DCO clock frequency control   | DCOCTL  | 056h  |
| <b>Port P2</b>               | Port P2 selection             | P2SEL   | 02Eh  |
|                              | Port P2 interrupt enable      | P2IE    | 02Dh  |
|                              | Port P2 interrupt edge select | P2IES   | 02Ch  |
|                              | Port P2 interrupt flag        | P2IFG   | 02Bh  |
|                              | Port P2 direction             | P2DIR   | 02Ah  |
|                              | Port P2 output                | P2OUT   | 029h  |
|                              | Port P2 input                 | P2IN    | 028h  |
| <b>Port P1</b>               | Port P1 selection             | P1SEL   | 026h  |
|                              | Port P1 interrupt enable      | P1IE    | 025h  |
|                              | Port P1 interrupt edge select | P1IES   | 024h  |
|                              | Port P1 interrupt flag        | P1IFG   | 023h  |
|                              | Port P1 direction             | P1DIR   | 022h  |
|                              | Port P1 output                | P1OUT   | 021h  |
|                              | Port P1 input                 | P1IN    | 020h  |
| <b>Special Function</b>      | SFR interrupt flag 2          | IFG2    | 003h  |
|                              | SFR interrupt flag 1          | IFG1    | 002h  |
|                              | SFR interrupt enable 2        | IE2     | 001h  |
|                              | SFR interrupt enable 1        | IE1     | 000h  |



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## absolute maximum ratings†

|  |                          |
|--|--------------------------|
| Voltage applied at $V_{CC}$ to $V_{SS}$ .....              | -0.3 V to 4.1 V          |
| Voltage applied to any pin (see Note) .....                | -0.3 V to $V_{CC}+0.3$ V |
| Diode current at any device terminal .....                 | $\pm 2$ mA               |
| Storage temperature, $T_{stg}$ (unprogrammed device) ..... | -55°C to 150°C           |
| Storage temperature, $T_{stg}$ (programmed device) .....   | -40°C to 85°C            |

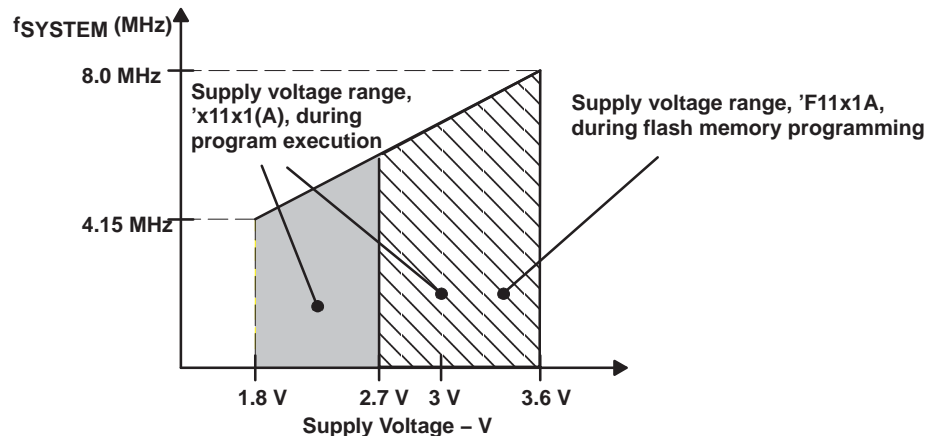
† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE: All voltages referenced to  $V_{SS}$ . The JTAG fuse-blow voltage,  $V_{FB}$ , is allowed to exceed the absolute maximum rating. The voltage is applied to the TEST pin when blowing the JTAG fuse.

## recommended operating conditions

|  |                                     | MIN               | NOM   | MAX  | UNITS |
|--|-------------------------------------|-------------------|-------|------|-------|
| Supply voltage during program execution, $V_{CC}$ (see Note 1) | MSP430C11x1                         | 1.8               |       | 3.6  | V     |
|  | MSP430F11x1A                        | 1.8               |       | 3.6  |       |
| Supply voltage during program/erase flash memory, $V_{CC}$     | MSP430F11x1A                        | 2.7               |       | 3.6  | V     |
| Supply voltage, $V_{SS}$                                       |                                     |                   | 0     |      | V     |
| Operating free-air temperature range, $T_A$                    | MSP430x11x1(A)                      | -40               |       | 85   | °C    |
| LFXT1 crystal frequency, $f_{(LFXT1)}$ (see Note 1 & 2)        | LF mode selected, XTS=0             | Watch crystal     | 32768 |      | Hz    |
|  |                                     | Ceramic resonator | 450   | 8000 | kHz   |
|  | XT1 mode selected, XTS=1            | Crystal           | 1000  | 8000 |       |
| Processor frequency $f_{(system)}$ (MCLK signal)               | $V_{CC} = 1.8$ V,<br>MSP430x11x1(A) | dc                |       | 4.15 | MHz   |
|  | $V_{CC} = 3.6$ V,<br>MSP430x11x1(A) | dc                |       | 8    |       |

- NOTES: 1. In LF mode, the LFXT1 oscillator requires a watch crystal. A 5.1M $\Omega$  resistor from XOUT to  $V_{SS}$  is recommended when  $V_{CC} < 2.5$  V. In XT1 mode, the LFXT1 and XT2 oscillators accept a ceramic resonator or crystal up to 4.15MHz at  $V_{CC} \geq 2.2$  V. In XT1 mode, the LFXT1 and XT2 oscillators accept a ceramic resonator or crystal up to 8MHz at  $V_{CC} \geq 2.8$  V.  
2. In LF mode, the LFXT1 oscillator requires a watch crystal. In XT1 mode, LFXT1 accepts a ceramic resonator or a crystal.



NOTE: Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum  $V_{CC}$  of 2.7 V.

**Figure 1. Frequency vs Supply Voltage, MSP430x11x1(A)**

# MSP430C11x1, MSP430F11x1A MIXED SIGNAL MICROCONTROLLER

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

supply current (into  $V_{CC}$ ) excluding external current

| PARAMETER      |  | TEST CONDITIONS   |  | MIN                          | TYP                       | MAX                          | UNIT                     |     |
|----------------|--|---|--|------------------------------|---------------------------|------------------------------|--------------------------|-----|
| $I_{(AM)}$     | Active mode  | C11x1   | $T_A = -40^\circ\text{C to } +85^\circ\text{C},$<br>$f_{(MCLK)} = f_{(SMCLK)} = 1 \text{ MHz},$<br>$f_{(ACLK)} = 32,768 \text{ Hz}$                  | $V_{CC} = 2.2 \text{ V}$     | 160                       | 200                          | $\mu\text{A}$            |     |
|                |  |   |  | $V_{CC} = 3 \text{ V}$       | 240                       | 300                          |                          |     |
|                | F11x1A   | $T_A = -40^\circ\text{C to } +85^\circ\text{C},$<br>$f_{(MCLK)} = f_{(SMCLK)} = f_{(ACLK)} = 4096 \text{ Hz}$   | $V_{CC} = 2.2 \text{ V}$   | 1.3                          | 2                         |                              |                          |     |
|                |  |   | $V_{CC} = 3 \text{ V}$   | 2.5                          | 3.2                       |                              |                          |     |
|                | F11x1A   | $T_A = -40^\circ\text{C to } +85^\circ\text{C},$<br>$f_{(MCLK)} = f_{(SMCLK)} = 1 \text{ MHz},$<br>$f_{(ACLK)} = 32,768 \text{ Hz},$<br>Program executes in flash             | $V_{CC} = 2.2 \text{ V}$   | 200                          | 250                       |                              |                          |     |
|                |  |   | $V_{CC} = 3 \text{ V}$   | 300                          | 350                       |                              |                          |     |
| F11x1A         | $T_A = -40^\circ\text{C to } +85^\circ\text{C},$<br>Program executes in flash<br>$f_{(MCLK)} = f_{(SMCLK)} = f_{(ACLK)} = 4096 \text{ Hz}$ | $V_{CC} = 2.2 \text{ V}$  | 3  | 5                            |                           |                              |                          |     |
|                |  | $V_{CC} = 3 \text{ V}$  | 11   | 18                           |                           |                              |                          |     |
| $I_{(CPUOff)}$ | Low-power mode,<br>(LPM0)  | C11x1   | $T_A = -40^\circ\text{C to } +85^\circ\text{C},$<br>$f_{(MCLK)} = 0, f_{(SMCLK)} = 1 \text{ MHz},$<br>$f_{(ACLK)} = 32,768 \text{ Hz}$               | $V_{CC} = 2.2 \text{ V}$     | 30                        | 40                           | $\mu\text{A}$            |     |
|                |  |   |  | $V_{CC} = 3 \text{ V}$       | 51                        | 60                           |                          |     |
|                | F11x1A   | $T_A = -40^\circ\text{C to } +85^\circ\text{C},$<br>$f_{(MCLK)} = 0, f_{(SMCLK)} = 1 \text{ MHz},$<br>$f_{(ACLK)} = 32,768 \text{ Hz}$  | $V_{CC} = 2.2 \text{ V}$   | 32                           | 45                        |                              |                          |     |
|                |  |   | $V_{CC} = 3 \text{ V}$   | 55                           | 70                        |                              |                          |     |
| $I_{(LPM2)}$   | Low-power mode,<br>(LPM2)  | C11x1   | $T_A = -40^\circ\text{C to } +85^\circ\text{C},$<br>$f_{(MCLK)} = f_{(SMCLK)} = 0 \text{ MHz},$<br>$f_{(ACLK)} = 32,768 \text{ Hz}, \text{SCG0} = 0$ | $V_{CC} = 2.2 \text{ V}$     | 11                        | 14                           | $\mu\text{A}$            |     |
|                |  |   |  | $V_{CC} = 3 \text{ V}$       | 17                        | 22                           |                          |     |
| $I_{(LPM3)}$   | Low-power mode,<br>(LPM3)  | C11x1   | $T_A = -40^\circ\text{C to } +85^\circ\text{C},$<br>$f_{(MCLK)} = f_{(SMCLK)} = 0 \text{ MHz},$<br>$f_{(ACLK)} = 32,768 \text{ Hz}, \text{SCG0} = 1$ | $V_{CC} = 2.2 \text{ V}$     | 1.2                       | 1.7                          | $\mu\text{A}$            |     |
|                |  |   |  | $V_{CC} = 3 \text{ V}$       | 2                         | 2.7                          |                          |     |
|                | F11x1A   | $T_A = -40^\circ\text{C to } +85^\circ\text{C},$<br>$f_{(MCLK)} = 0 \text{ MHz},$<br>$f_{(SMCLK)} = 0 \text{ MHz},$<br>$f_{(ACLK)} = 32,768 \text{ Hz},$<br>$\text{SCG0} = 1$ | $T_A = -40^\circ\text{C}$  | $V_{CC} = 2.2 \text{ V}$     | 0.8                       | 1.2                          |                          |     |
|                |  |   | $T_A = 25^\circ\text{C}$   |                              | 0.7                       | 1                            |                          |     |
|                |  |   | $T_A = 85^\circ\text{C}$   | $V_{CC} = 3 \text{ V}$       | 1.6                       | 2.3                          |                          |     |
|                |  |   | $T_A = -40^\circ\text{C}$  |                              | 1.8                       | 2.2                          |                          |     |
|                |  |   | $T_A = 25^\circ\text{C}$   | 1.6                          | 1.9                       |                              |                          |     |
|                |  |   | $T_A = 85^\circ\text{C}$   | 2.3                          | 3.4                       |                              |                          |     |
| $I_{(LPM4)}$   | Low-power mode,<br>(LPM4)  | C11x1   | $f_{(MCLK)} = 0 \text{ MHz},$<br>$f_{(SMCLK)} = 0 \text{ MHz},$<br>$f_{(ACLK)} = 0 \text{ Hz}, \text{SCG0} = 1$                                      | $V_{CC} = 2.2 \text{ V/3 V}$ | $T_A = -40^\circ\text{C}$ | 0.1                          | 0.5                      |     |
|                |  |   |  |                              | $T_A = 25^\circ\text{C}$  | 0.1                          | 0.5                      |     |
|                |  |   |  | F11x1A                       | $T_A = -40^\circ\text{C}$ | $V_{CC} = 2.2 \text{ V/3 V}$ | 0.1                      | 0.5 |
|                |  |   |  |                              |                           |                              | $T_A = 25^\circ\text{C}$ | 0.1 |
|                | F11x1A   | $T_A = -40^\circ\text{C}$   | $V_{CC} = 2.2 \text{ V/3 V}$   | 0.1                          | 0.5                       |                              |                          |     |
|                |  |   |  | $T_A = 25^\circ\text{C}$     | 0.1                       | 0.5                          |                          |     |
|                | F11x1A   | $T_A = -40^\circ\text{C}$   | $V_{CC} = 2.2 \text{ V/3 V}$   | 0.1                          | 0.5                       |                              |                          |     |
|                |  |   |  | $T_A = 25^\circ\text{C}$     | 0.1                       | 0.5                          |                          |     |

NOTE: All inputs are tied to 0 V or  $V_{CC}$ . Outputs do not source or sink any current.

current consumption of active mode versus system frequency, C version, F version

$$I_{AM} = I_{AM}[1 \text{ MHz}] \times f_{\text{system}} [\text{MHz}]$$

current consumption of active mode versus supply voltage, C version

$$I_{AM} = I_{AM}[3 \text{ V}] + 105 \mu\text{A/V} \times (V_{CC} - 3 \text{ V})$$

current consumption of active mode versus supply voltage, F version

$$I_{AM} = I_{AM}[3 \text{ V}] + 120 \mu\text{A/V} \times (V_{CC} - 3 \text{ V})$$



electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

**Schmitt-trigger inputs – Ports P1 and P2; (P1.0 to P1.7, P2.0 to P2.5)**

| PARAMETER        |   | TEST CONDITIONS         | MIN | TYP | MAX | UNIT |
|------------------|---|-------------------------|-----|-----|-----|------|
| V <sub>IT+</sub> | Positive-going input threshold voltage                          | V <sub>CC</sub> = 2.2 V | 1.1 |     | 1.5 | V    |
|                  |   | V <sub>CC</sub> = 3 V   | 1.5 |     | 1.9 |      |
| V <sub>IT-</sub> | Negative-going input threshold voltage                          | V <sub>CC</sub> = 2.2 V | 0.4 |     | 0.9 | V    |
|                  |   | V <sub>CC</sub> = 3 V   | 0.9 |     | 1.3 |      |
| V <sub>hys</sub> | Input voltage hysteresis (V <sub>IT+</sub> – V <sub>IT-</sub> ) | V <sub>CC</sub> = 2.2 V | 0.3 |     | 1.1 | V    |
|                  |   | V <sub>CC</sub> = 3 V   | 0.5 |     | 1   |      |

**standard inputs –  $\overline{\text{RST}}/\text{NMI}$ , JTAG: TCK, TMS, TDI/TCLK**

| PARAMETER       |                          | TEST CONDITIONS               | MIN                 | TYP | MAX                  | UNIT |
|-----------------|--------------------------|-------------------------------|---------------------|-----|----------------------|------|
| V <sub>IL</sub> | Low-level input voltage  | V <sub>CC</sub> = 2.2 V / 3 V | V <sub>SS</sub>     |     | V <sub>SS</sub> +0.6 | V    |
| V <sub>IH</sub> | High-level input voltage |                               | 0.8×V <sub>CC</sub> |     | V <sub>CC</sub>      | V    |

**inputs Px.x, TA<sub>x</sub>**

| PARAMETER            |   | TEST CONDITIONS   | V <sub>CC</sub> | MIN | TYP | MAX | UNIT  |
|----------------------|---|---|-----------------|-----|-----|-----|-------|
| t <sub>(int)</sub>   | External interrupt timing                         | Port P1, P2: P1.x to P2.x, External trigger signal for the interrupt flag, (see Note 1) | 2.2 V/3 V       | 1.5 |     |     | cycle |
|                      |   |   | 2.2 V           | 62  |     |     | ns    |
|                      |   |   | 3 V             | 50  |     |     |       |
| t <sub>(cap)</sub>   | Timer_A, capture timing                           | TA0, TA1, TA2   | 2.2 V           | 62  |     |     | ns    |
|                      |   |   | 3 V             | 50  |     |     |       |
| f <sub>(TAext)</sub> | Timer_A clock frequency externally applied to pin | TACLK, INCLK t <sub>(H)</sub> = t <sub>(L)</sub>  | 2.2 V           |     |     | 8   | MHz   |
|                      |   |   | 3 V             |     |     | 10  |       |
| f <sub>(TAint)</sub> | Timer_A clock frequency                           | SMCLK or ACLK signal selected   | 2.2 V           |     |     | 8   | MHz   |
|                      |   |   | 3 V             |     |     | 10  |       |

NOTES: 1. The external signal sets the interrupt flag every time the minimum t<sub>(int)</sub> cycle and time parameters are met. It may be set even with trigger signals shorter than t<sub>(int)</sub>. Both the cycle and timing specifications must be met to ensure the flag is set. t<sub>(int)</sub> is measured in MCLK cycles.

**leakage current**

| PARAMETER               |                                | TEST CONDITIONS                           | MIN                          | TYP | MAX | UNIT |
|-------------------------|--------------------------------|---|------------------------------|-----|-----|------|
| I <sub>lkg</sub> (Px.x) | High-impedance leakage current | Port P1: P1.x, 0 ≤ x ≤ 7 (see Notes 1, 2) | V <sub>CC</sub> = 2.2 V/3 V, |     | ±50 | nA   |
|                         |                                | Port P2: P2.x, 0 ≤ x ≤ 5 (see Notes 1, 2) | V <sub>CC</sub> = 2.2 V/3 V, |     | ±50 |      |

NOTES: 1. The leakage current is measured with V<sub>SS</sub> or V<sub>CC</sub> applied to the corresponding pin(s), unless otherwise noted.  
2. The leakage of the digital port pins is measured individually. The port pin must be selected for input and there must be no optional pullup or pulldown resistor.

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

## outputs – Ports P1 and P2; (P1.0 to P1.7, P2.0 to P2.5)

| PARAMETER       |   | TEST CONDITIONS    |                         |            | MIN                   | TYP                   | MAX             | UNIT |
|-----------------|---|--------------------|-------------------------|------------|-----------------------|-----------------------|-----------------|------|
| V <sub>OH</sub> | High-level output voltage<br>Port 1 and Port 2 (C11x1)<br>Port 1 (F11x1A) | I(OHmax) = -1.5 mA | V <sub>CC</sub> = 2.2 V | See Note 1 | V <sub>CC</sub> -0.25 |                       | V <sub>CC</sub> | V    |
|                 |   | I(OHmax) = -6 mA   |                         | See Note 2 | V <sub>CC</sub> -0.6  | V <sub>CC</sub>       |                 |      |
|                 |   | I(OHmax) = -1.5 mA | V <sub>CC</sub> = 3 V   | See Note 1 | V <sub>CC</sub> -0.25 |                       | V <sub>CC</sub> |      |
|                 |   | I(OHmax) = -6 mA   |                         | See Note 2 | V <sub>CC</sub> -0.6  | V <sub>CC</sub>       |                 |      |
| V <sub>OH</sub> | High-level output voltage<br>Port 2 (F11x1A)                              | I(OHmax) = -1 mA   | V <sub>CC</sub> = 2.2 V | See Note 3 | V <sub>CC</sub> -0.25 |                       | V <sub>CC</sub> | V    |
|                 |   | I(OHmax) = -3.4 mA |                         | See Note 3 | V <sub>CC</sub> -0.6  | V <sub>CC</sub>       |                 |      |
|                 |   | I(OHmax) = -1 mA   | V <sub>CC</sub> = 3 V   | See Note 3 | V <sub>CC</sub> -0.25 |                       | V <sub>CC</sub> |      |
|                 |   | I(OHmax) = -3.4 mA |                         | See Note 3 | V <sub>CC</sub> -0.6  | V <sub>CC</sub>       |                 |      |
| V <sub>OL</sub> | Low-level output voltage<br>Port 1 and Port 2 (C11x1,<br>F11x1A)          | I(OLmax) = 1.5 mA  | V <sub>CC</sub> = 2.2 V | See Note 1 | V <sub>SS</sub>       | V <sub>SS</sub> +0.25 | V               |      |
|                 |   | I(OLmax) = 6 mA    |                         | See Note 2 | V <sub>SS</sub>       | V <sub>SS</sub> +0.6  |                 |      |
|                 |   | I(OLmax) = 1.5 mA  | V <sub>CC</sub> = 3 V   | See Note 1 | V <sub>SS</sub>       | V <sub>SS</sub> +0.25 |                 |      |
|                 |   | I(OLmax) = 6 mA    |                         | See Note 2 | V <sub>SS</sub>       | V <sub>SS</sub> +0.6  |                 |      |

- NOTES: 1. The maximum total current, I<sub>OHmax</sub> and I<sub>OLmax</sub>, for all outputs combined, should not exceed ±12 mA to hold the maximum voltage drop specified.  
 2. The maximum total current, I<sub>OHmax</sub> and I<sub>OLmax</sub>, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.  
 3. One output loaded at a time.

## output frequency

| PARAMETER                                |                             | TEST CONDITIONS   |  |           | VCC           | MIN           | TYP                 | MAX           | UNIT |
|--|-----------------------------|---|--|-----------|---------------|---------------|---------------------|---------------|------|
| f <sub>P20</sub>                         | Output frequency            | P2.0/ACLK, C <sub>L</sub> = 20 pF   |  |           | 2.2 V/3 V     |               | f <sub>System</sub> |               | MHz  |
| f <sub>Tax</sub>                         |                             | TA0, TA1, TA2, C <sub>L</sub> = 20 pF<br>Internal clock source, SMCLK signal applied (see Note 1) |  |           | 2.2 V/3 V     | dc            | f <sub>System</sub> |               |      |
| t <sub>Xdc</sub>                         | Duty cycle of O/P frequency | P1.4/SMCLK,<br>C <sub>L</sub> = 20 pF   | f <sub>SMCLK</sub> = f <sub>LFXT1</sub> = f <sub>XT1</sub> |           | 2.2 V/3 V     | 40%           |                     | 60%           |      |
|  |                             |   | f <sub>SMCLK</sub> = f <sub>LFXT1</sub> = f <sub>LF</sub>  |           |               | 35%           |                     | 65%           |      |
|  |                             |   | f <sub>SMCLK</sub> = f <sub>LFXT1</sub> /n                 |           |               | 50%–<br>15 ns | 50%                 | 50%+<br>15 ns |      |
|  |                             | f <sub>SMCLK</sub> = f <sub>DCOCLK</sub>  |  | 2.2 V/3 V | 50%–<br>15 ns | 50%           | 50%+<br>15 ns       |               |      |
|  |                             | P2.0/ACLK,<br>C <sub>L</sub> = 20 pF  | f <sub>P20</sub> = f <sub>LFXT1</sub> = f <sub>XT1</sub>   |           | 2.2 V/3 V     | 40%           |                     | 60%           |      |
|  |                             |   | f <sub>P20</sub> = f <sub>LFXT1</sub> = f <sub>LF</sub>    |           |               | 30%           |                     | 70%           |      |
| f <sub>P20</sub> = f <sub>LFXT1</sub> /n |                             |   |  | 50%       |               |               |                     |               |      |
| t <sub>TAdc</sub>                        |                             | TA0, TA1, TA2, C <sub>L</sub> = 20 pF, duty cycle = 50%   |  |           | 2.2 V/3 V     |               | 0                   | ±50           | ns   |

NOTE 1: The limits of the system clock MCLK has to be met. MCLK and SMCLK can have different frequencies.



electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)  
outputs – Ports P1 and P2 (continued)

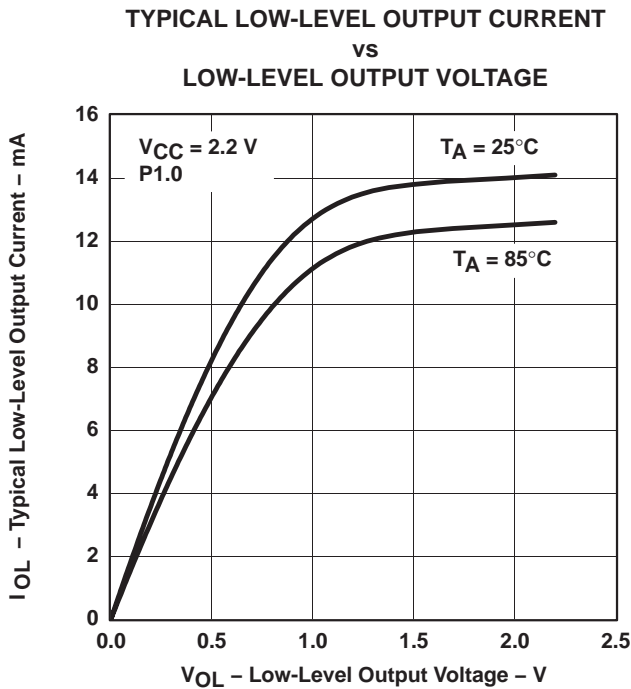


Figure 2

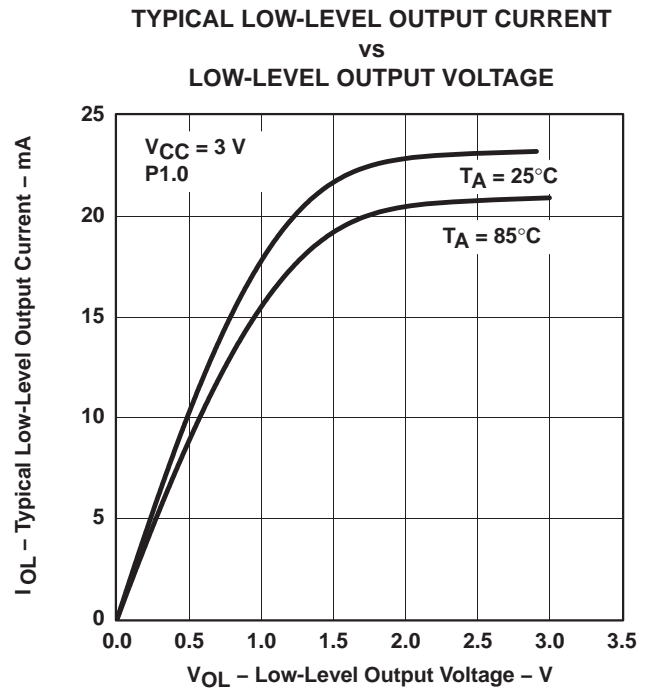


Figure 3

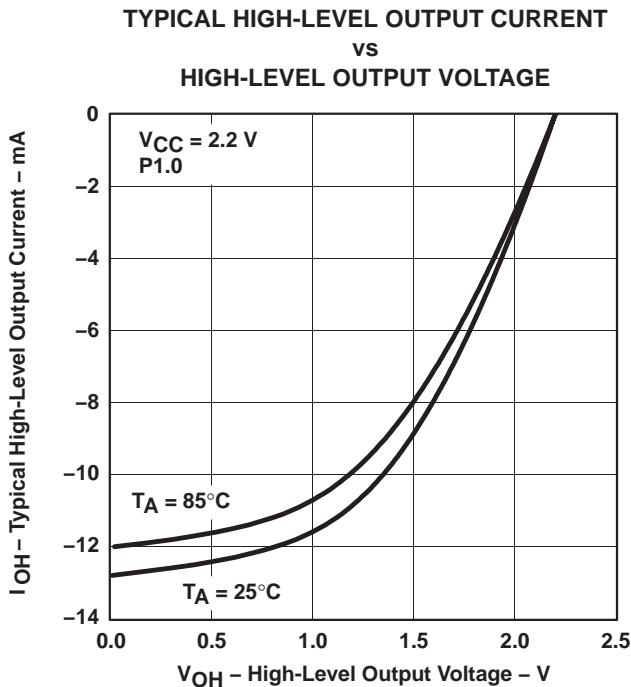


Figure 4

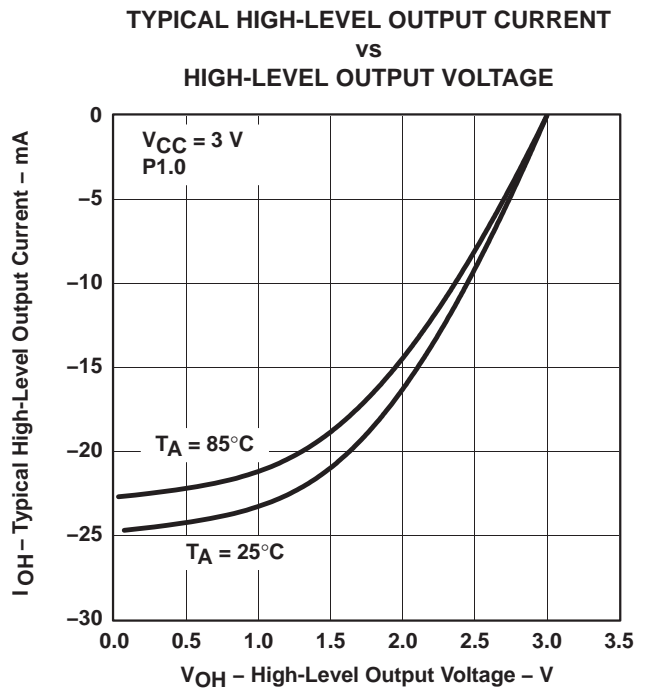


Figure 5

NOTE: One output loaded at a time.

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

optional resistors, individually programmable with ROM code (see Note 1)

| PARAMETER            |  | TEST CONDITIONS             | MIN  | TYP | MAX | UNIT |
|----------------------|--|-----------------------------|------|-----|-----|------|
| R <sub>(opt1)</sub>  | Resistors, individually programmable with ROM code, all port pins, values applicable for pulldown and pullup | V <sub>CC</sub> = 2.2 V/3 V | 2.5  | 5   | 10  | kΩ   |
| R <sub>(opt2)</sub>  |  |                             | 3.8  | 7.7 | 15  | kΩ   |
| R <sub>(opt3)</sub>  |  |                             | 7.6  | 15  | 31  | kΩ   |
| R <sub>(opt4)</sub>  |  |                             | 11.5 | 23  | 46  | kΩ   |
| R <sub>(opt5)</sub>  |  |                             | 23   | 45  | 90  | kΩ   |
| R <sub>(opt6)</sub>  |  |                             | 46   | 90  | 180 | kΩ   |
| R <sub>(opt7)</sub>  |  |                             | 70   | 140 | 280 | kΩ   |
| R <sub>(opt8)</sub>  |  |                             | 115  | 230 | 460 | kΩ   |
| R <sub>(opt9)</sub>  |  |                             | 160  | 320 | 640 | kΩ   |
| R <sub>(opt10)</sub> |  |                             | 205  | 420 | 830 | kΩ   |

NOTE 1: Optional resistors R<sub>Optx</sub> for pulldown or pullup are not available in standard flash memory device MSP430F11x1A.

wake-up from lower power modes (LPMx)

| PARAMETER           |                         | TEST CONDITIONS  | MIN | TYP | MAX | UNIT |
|---------------------|-------------------------|--|-----|-----|-----|------|
| t <sub>(LPM0)</sub> | Delay time (see Note 1) | V <sub>CC</sub> = 2.2 V/3 V                              |     | 100 |     | ns   |
| t <sub>(LPM2)</sub> |                         | V <sub>CC</sub> = 2.2 V/3 V                              |     | 100 |     |      |
| t <sub>(LPM3)</sub> |                         | f <sub>(MCLK)</sub> = 1 MHz, V <sub>CC</sub> = 2.2 V/3 V |     |     | 6   | μs   |
|                     |                         | f <sub>(MCLK)</sub> = 2 MHz, V <sub>CC</sub> = 2.2 V/3 V |     |     | 6   |      |
|                     |                         | f <sub>(MCLK)</sub> = 3 MHz, V <sub>CC</sub> = 2.2 V/3 V |     |     | 6   |      |
| t <sub>(LPM4)</sub> |                         | f <sub>(MCLK)</sub> = 1 MHz, V <sub>CC</sub> = 2.2 V/3 V |     |     | 6   | μs   |
|                     |                         | f <sub>(MCLK)</sub> = 2 MHz, V <sub>CC</sub> = 2.2 V/3 V |     |     | 6   |      |
|                     |                         | f <sub>(MCLK)</sub> = 3 MHz, V <sub>CC</sub> = 2.2 V/3 V |     |     | 6   |      |

NOTE 1: Parameter applicable only if DCOCLK is used for MCLK.

## RAM

| PARAMETER           |                         | MIN | NOM | MAX | UNIT |
|---------------------|-------------------------|-----|-----|-----|------|
| V <sub>(RAMh)</sub> | CPU halted (see Note 1) | 1.6 |     |     | V    |

NOTE 1: This parameter defines the minimum supply voltage V<sub>CC</sub> when the data in the program memory RAM remains unchanged. No program execution should happen during this supply voltage condition.



**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)**

**Comparator\_A (see Note 1)**

| PARAMETER                         |   | TEST CONDITIONS  | MIN                         | TYP | MAX  | UNIT               |      |    |
|-----------------------------------|---|--|-----------------------------|-----|------|--------------------|------|----|
| I <sub>(DD)</sub>                 |   | CAON=1, CARSEL=0, CAREF=0  | V <sub>CC</sub> = 2.2 V     | 25  | 40   | μA                 |      |    |
|                                   |   |  | V <sub>CC</sub> = 3 V       | 45  | 60   |                    |      |    |
| I <sub>(Refladder/RefDiode)</sub> |   | CAON=1, CARSEL=0, CAREF=1/2/3, no load at P2.3/CA0/TA1 and P2.4/CA1/TA2                    | V <sub>CC</sub> = 2.2 V     | 30  | 50   | μA                 |      |    |
|                                   |   |  | V <sub>CC</sub> = 3 V       | 45  | 71   |                    |      |    |
| V <sub>(IC)</sub>                 | Common-mode input voltage                                   | CAON =1  | V <sub>CC</sub> = 2.2 V/3 V |     | 0    | V <sub>CC</sub> -1 | V    |    |
| V <sub>(Ref025)</sub>             | $\frac{\text{Voltage @ } 0.25 V_{CC} \text{ node}}{V_{CC}}$ | PCA0=1, CARSEL=1, CAREF=1, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2                        | V <sub>CC</sub> = 2.2 V/3 V |     | 0.23 | 0.24               | 0.25 |    |
| V <sub>(Ref050)</sub>             | $\frac{\text{Voltage @ } 0.5 V_{CC} \text{ node}}{V_{CC}}$  | PCA0=1, CARSEL=1, CAREF=2, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2                        | V <sub>CC</sub> = 2.2 V/3 V |     | 0.47 | 0.48               | 0.5  |    |
| V <sub>(RefVT)</sub>              | (see Figure 6 and Figure 7)                                 | PCA0=1, CARSEL=1, CAREF=3, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2, T <sub>A</sub> = 85°C | V <sub>CC</sub> = 2.2 V     | 390 | 480  | 540                | mV   |    |
|                                   |   |  | V <sub>CC</sub> = 3 V       | 400 | 490  | 550                |      |    |
| V <sub>(offset)</sub>             | Offset voltage  | See Note 2   | V <sub>CC</sub> = 2.2 V/3 V |     | -30  | 30                 | mV   |    |
| V <sub>hys</sub>                  | Input hysteresis  | CAON=1   | V <sub>CC</sub> = 2.2 V/3 V |     | 0    | 0.7                | 1.4  | mV |
| t <sub>(response LH)</sub>        |   | T <sub>A</sub> = 25°C, Overdrive 10 mV, Without filter: CAF=0                              | V <sub>CC</sub> = 2.2 V     | 160 | 210  | 300                | ns   |    |
|                                   |   |  | V <sub>CC</sub> = 3 V       | 90  | 150  | 240                |      |    |
|                                   |   | T <sub>A</sub> = 25°C, Overdrive 10 mV, With filter: CAF=1                                 | V <sub>CC</sub> = 2.2 V     | 1.4 | 1.9  | 3.4                | μs   |    |
|                                   |   |  | V <sub>CC</sub> = 3 V       | 0.9 | 1.5  | 2.6                |      |    |
| t <sub>(response HL)</sub>        |   | T <sub>A</sub> = 25°C, Overdrive 10 mV, Without filter: CAF=0                              | V <sub>CC</sub> = 2.2 V     | 130 | 210  | 300                | ns   |    |
|                                   |   |  | V <sub>CC</sub> = 3 V       | 80  | 150  | 240                |      |    |
|                                   |   | T <sub>A</sub> = 25°C, Overdrive 10 mV, With filter: CAF=1                                 | V <sub>CC</sub> = 2.2 V     | 1.4 | 1.9  | 3.4                | μs   |    |
|                                   |   |  | V <sub>CC</sub> = 3 V       | 0.9 | 1.5  | 2.6                |      |    |

- NOTES: 1. The leakage current for the Comparator\_A terminals is identical to I<sub>kg(Px.x)</sub> specification.  
 2. The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator\_A inputs on successive measurements. The two successive measurements are then summed together.

# MSP430C11x1, MSP430F11x1A MIXED SIGNAL MICROCONTROLLER

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

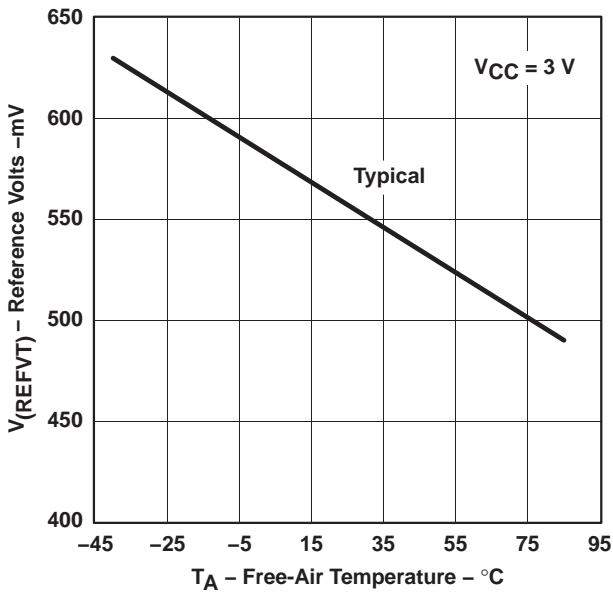


Figure 6. V(REFVT) vs Temperature, V<sub>CC</sub> = 3 V

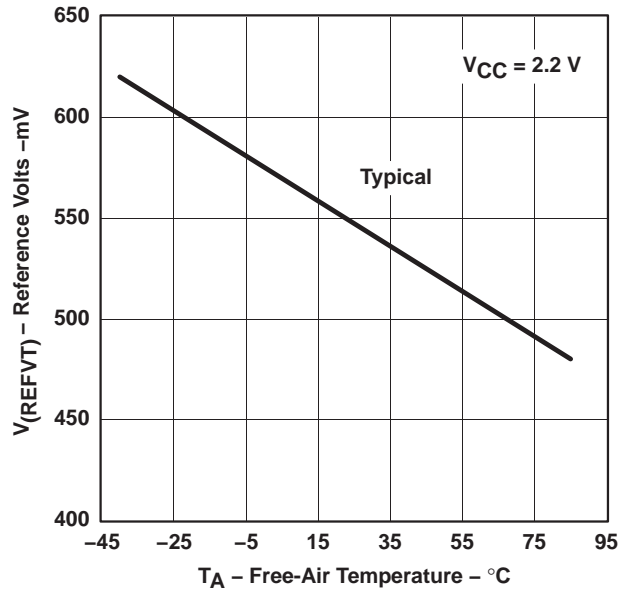


Figure 7. V(REFVT) vs Temperature, V<sub>CC</sub> = 2.2 V

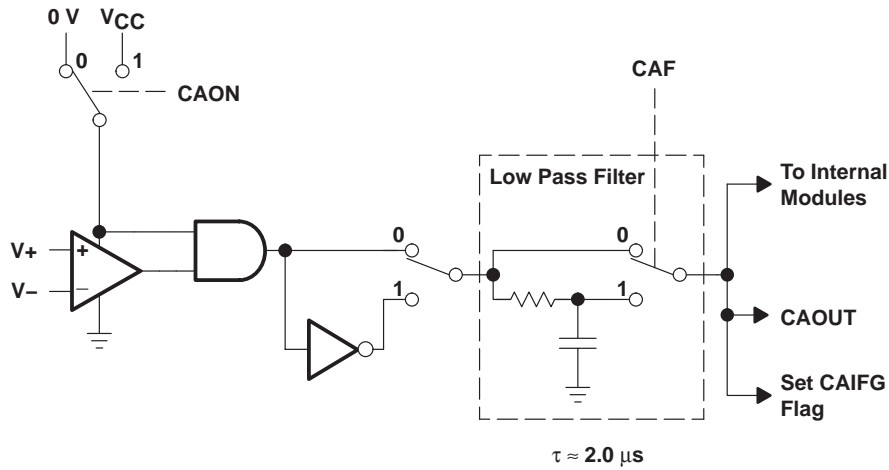


Figure 8. Block Diagram of Comparator\_A Module

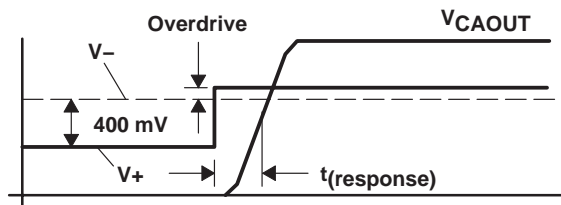


Figure 9. Overdrive Definition

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

PUC/POR

| PARAMETER          | TEST CONDITIONS  | MIN                          | TYP | MAX | UNIT    |   |
|--------------------|--|------------------------------|-----|-----|---------|---|
| $t_{(POR\_Delay)}$ | Internal time delay to release POR                                     |                              | 150 | 250 | $\mu s$ |   |
| $V_{POR}$          | $V_{CC}$ threshold at which POR release delay time begins (see Note 1) | $T_A = -40^\circ C$          |     | 1.4 | 1.8     | V |
|                    |  | $T_A = 25^\circ C$           |     | 1.1 | 1.5     | V |
|                    |  | $T_A = 85^\circ C$           |     | 0.8 | 1.2     | V |
| $V_{(min)}$        | $V_{CC}$ threshold required to generate a POR (see Note 2)             | $V_{CC}  dV/dt  \geq 1V/ms$  |     |     | V       |   |
| $t_{(reset)}$      | $\overline{RST}/NMI$ low time for PUC/POR                              | Reset is accepted internally |     | 2   | $\mu s$ |   |

- NOTES: 1.  $V_{CC}$  rise time  $dV/dt \geq 1V/ms$ .  
 2. When driving  $V_{CC}$  low in order to generate a POR condition,  $V_{CC}$  should be driven to 200mV or lower with a  $dV/dt$  equal to or less than  $-1V/ms$ . The corresponding rising  $V_{CC}$  must also meet the  $dV/dt$  requirement equal to or greater than  $+1V/ms$ .

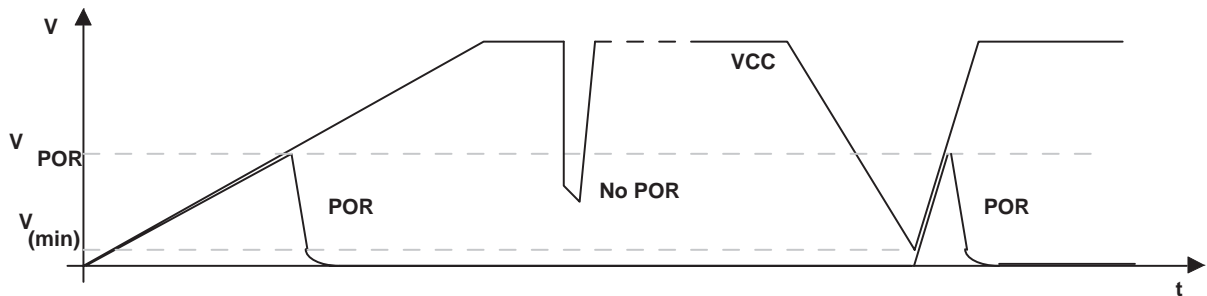


Figure 10. Power-On Reset (POR) vs Supply Voltage

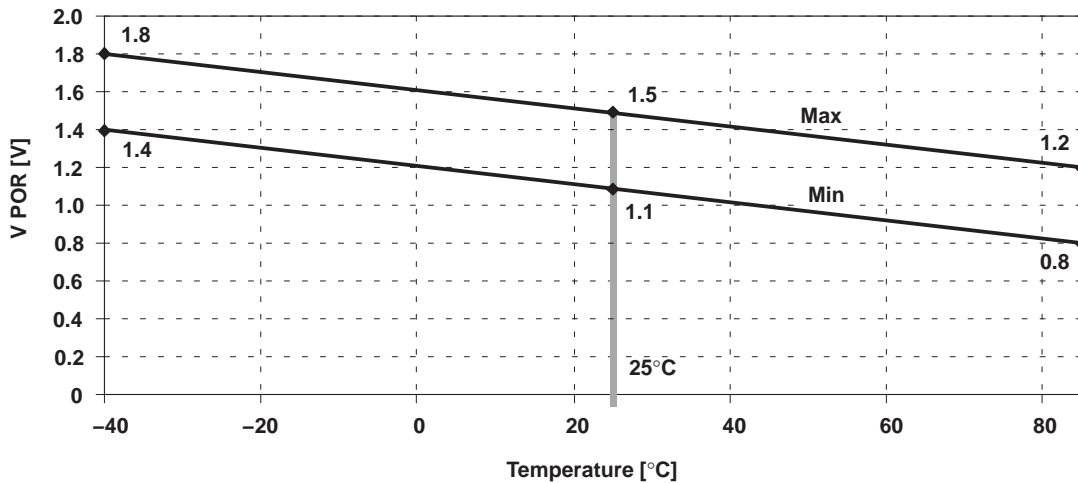


Figure 11.  $V_{POR}$  vs Temperature

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

## DCO

| PARAMETER      | TEST CONDITIONS  | MIN                         | TYP                        | MAX                        | UNIT                       |       |
|----------------|--|-----------------------------|----------------------------|----------------------------|----------------------------|-------|
| f(DCO03)       | R <sub>sel</sub> = 0, DCO = 3, MOD = 0, DCOR = 0, T <sub>A</sub> = 25°C                      | V <sub>CC</sub> = 2.2 V     | 0.08                       | 0.12                       | 0.15                       | MHz   |
|                |  | V <sub>CC</sub> = 3 V       | 0.08                       | 0.13                       | 0.16                       |       |
| f(DCO13)       | R <sub>sel</sub> = 1, DCO = 3, MOD = 0, DCOR = 0, T <sub>A</sub> = 25°C                      | V <sub>CC</sub> = 2.2 V     | 0.14                       | 0.19                       | 0.23                       | MHz   |
|                |  | V <sub>CC</sub> = 3 V       | 0.14                       | 0.18                       | 0.22                       |       |
| f(DCO23)       | R <sub>sel</sub> = 2, DCO = 3, MOD = 0, DCOR = 0, T <sub>A</sub> = 25°C                      | V <sub>CC</sub> = 2.2 V     | 0.22                       | 0.30                       | 0.36                       | MHz   |
|                |  | V <sub>CC</sub> = 3 V       | 0.22                       | 0.28                       | 0.34                       |       |
| f(DCO33)       | R <sub>sel</sub> = 3, DCO = 3, MOD = 0, DCOR = 0, T <sub>A</sub> = 25°C                      | V <sub>CC</sub> = 2.2 V     | 0.37                       | 0.49                       | 0.59                       | MHz   |
|                |  | V <sub>CC</sub> = 3 V       | 0.37                       | 0.47                       | 0.56                       |       |
| f(DCO43)       | R <sub>sel</sub> = 4, DCO = 3, MOD = 0, DCOR = 0, T <sub>A</sub> = 25°C                      | V <sub>CC</sub> = 2.2 V     | 0.61                       | 0.77                       | 0.93                       | MHz   |
|                |  | V <sub>CC</sub> = 3 V       | 0.61                       | 0.75                       | 0.9                        |       |
| f(DCO53)       | R <sub>sel</sub> = 5, DCO = 3, MOD = 0, DCOR = 0, T <sub>A</sub> = 25°C                      | V <sub>CC</sub> = 2.2 V     | 1                          | 1.2                        | 1.5                        | MHz   |
|                |  | V <sub>CC</sub> = 3 V       | 1                          | 1.3                        | 1.5                        |       |
| f(DCO63)       | R <sub>sel</sub> = 6, DCO = 3, MOD = 0, DCOR = 0, T <sub>A</sub> = 25°C                      | V <sub>CC</sub> = 2.2 V     | 1.6                        | 1.9                        | 2.2                        | MHz   |
|                |  | V <sub>CC</sub> = 3 V       | 1.69                       | 2                          | 2.29                       |       |
| f(DCO73)       | R <sub>sel</sub> = 7, DCO = 3, MOD = 0, DCOR = 0, T <sub>A</sub> = 25°C                      | V <sub>CC</sub> = 2.2 V     | 2.4                        | 2.9                        | 3.4                        | MHz   |
|                |  | V <sub>CC</sub> = 3 V       | 2.7                        | 3.2                        | 3.65                       |       |
| f(DCO77)       | R <sub>sel</sub> = 7, DCO = 7, MOD = 0, DCOR = 0, T <sub>A</sub> = 25°C                      | V <sub>CC</sub> = 2.2 V     | 4                          | 4.5                        | 4.9                        | MHz   |
|                |  | V <sub>CC</sub> = 3 V       | 4.4                        | 4.9                        | 5.4                        |       |
| f(DCO47)       | R <sub>sel</sub> = 4, DCO = 7, MOD = 0, DCOR = 0, T <sub>A</sub> = 25°C                      | V <sub>CC</sub> = 2.2 V/3 V | f <sub>DCO40</sub><br>x1.7 | f <sub>DCO40</sub><br>x2.1 | f <sub>DCO40</sub><br>x2.5 | MHz   |
| S(Rsel)        | S <sub>R</sub> = f <sub>Rsel+1</sub> /f <sub>Rsel</sub>                                      | V <sub>CC</sub> = 2.2 V/3 V | 1.35                       | 1.65                       | 2                          | ratio |
| S(DCO)         | S <sub>DCO</sub> = f <sub>DCO+1</sub> /f <sub>DCO</sub>                                      | V <sub>CC</sub> = 2.2 V/3 V | 1.07                       | 1.12                       | 1.16                       |       |
| D <sub>t</sub> | Temperature drift, R <sub>sel</sub> = 4, DCO = 3, MOD = 0<br>(see Note 1)                    | V <sub>CC</sub> = 2.2 V     | -0.31                      | -0.36                      | -0.40                      | %/°C  |
|                |  | V <sub>CC</sub> = 3 V       | -0.33                      | -0.38                      | -0.43                      |       |
| D <sub>V</sub> | Drift with V <sub>CC</sub> variation, R <sub>sel</sub> = 4, DCO = 3, MOD = 0<br>(see Note 1) | V <sub>CC</sub> = 2.2 V/3 V | 0                          | 5                          | 10                         | %/V   |

NOTE 1: These parameters are not production tested.

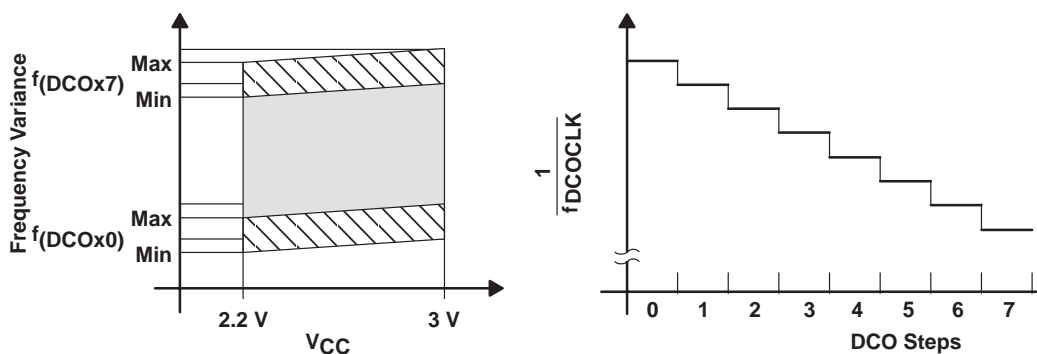


Figure 12. DCO Characteristics

**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)**

**main DCO characteristics**

- Individual devices have a minimum and maximum operation frequency. The specified parameters for  $f_{(DCOx0)}$  to  $f_{(DCOx7)}$  are valid for all devices.
- All ranges selected by Rsel(n) overlap with Rsel(n+1): Rsel0 overlaps Rsel1, ... Rsel6 overlaps Rsel7.
- DCO control bits DCO0, DCO1, and DCO2 have a step size as defined by parameter  $S_{DCO}$ .
- Modulation control bits MOD0 to MOD4 select how often  $f_{(DCO+1)}$  is used within the period of 32 DCOCLK cycles. The frequency  $f_{(DCO)}$  is used for the remaining cycles. The frequency is an average equal to:

$$f_{average} = \frac{32 \times f_{(DCO)} \times f_{(DCO+1)}}{MOD \times f_{(DCO)} + (32 - MOD) \times f_{(DCO+1)}}$$

**DCO when using  $R_{OSC}$  (see Note 1)**

| PARAMETER   | TEST CONDITIONS  | V <sub>CC</sub> | MIN | NOM      | MAX | UNIT |
|---|--|-----------------|-----|----------|-----|------|
| f <sub>DCO</sub> , DCO output frequency               | R <sub>sel</sub> = 4, DCO = 3, MOD = 0, DCOR = 1,<br>T <sub>A</sub> = 25°C | 2.2 V           |     | 1.8±15%  |     | MHz  |
|   |  | 3 V             |     | 1.95±15% |     | MHz  |
| D <sub>t</sub> , Temperature drift                    | R <sub>sel</sub> = 4, DCO = 3, MOD = 0, DCOR = 1                           | 2.2 V/3 V       |     | ±0.1     |     | %/°C |
| D <sub>v</sub> , Drift with V <sub>CC</sub> variation | R <sub>sel</sub> = 4, DCO = 3, MOD = 0, DCOR = 1                           | 2.2 V/3 V       |     | 10       |     | %/V  |

NOTES: 1.  $R_{OSC}$  = 100kΩ. Metal film resistor, type 0257. 0.6 watt with 1% tolerance and T<sub>K</sub> = ±50ppm/°C.

**crystal oscillator, LFXT1**

| PARAMETER                            | TEST CONDITIONS   | MIN                 | TYP | MAX                 | UNIT |
|--------------------------------------|---|---------------------|-----|---------------------|------|
| C <sub>XIN</sub> Input capacitance   | XTS=0; LF mode selected.<br>V <sub>CC</sub> = 2.2 V / 3 V               |                     | 12  |                     | pF   |
|                                      | XTS=1; XT1 mode selected.<br>V <sub>CC</sub> = 2.2 V / 3 V (see Note 1) |                     | 2   |                     |      |
| C <sub>XOUT</sub> Output capacitance | XTS=0; LF mode selected.<br>V <sub>CC</sub> = 2.2 V / 3 V               |                     | 12  |                     | pF   |
|                                      | XTS=1; XT1 mode selected.<br>V <sub>CC</sub> = 2.2 V / 3 V (see Note 1) |                     | 2   |                     |      |
| V <sub>IL</sub>                      | Input levels at XIN<br>V <sub>CC</sub> = 2.2 V/3 V (see Note 2)         | V <sub>SS</sub>     |     | 0.2×V <sub>CC</sub> | V    |
| V <sub>IH</sub>                      |   | 0.8×V <sub>CC</sub> |     | V <sub>CC</sub>     |      |

- NOTES: 1. Requires external capacitors at both terminals. Values are specified by crystal manufacturers.  
2. Applies only when using an external logic-level clock source. Not applicable when using a crystal or resonator.

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

## Flash Memory

| PARAMETER                   |   | TEST CONDITIONS       | V <sub>CC</sub> | MIN             | NOM             | MAX | UNIT             |
|-----------------------------|---|-----------------------|-----------------|-----------------|-----------------|-----|------------------|
| V <sub>CC</sub> (PGM/ERASE) | Program and Erase supply voltage                    |                       |                 | 2.7             |                 | 3.6 | V                |
| f <sub>FTG</sub>            | Flash Timing Generator frequency                    |                       |                 | 257             |                 | 476 | kHz              |
| I <sub>PGM</sub>            | Supply current from V <sub>CC</sub> during program  |                       | 2.7 V/ 3.6 V    |                 | 3               | 5   | mA               |
| I <sub>ERASE</sub>          | Supply current from V <sub>CC</sub> during erase    |                       | 2.7 V/ 3.6 V    |                 | 3               | 7   | mA               |
| t <sub>CPT</sub>            | Cumulative program time                             | see Note 1            | 2.7 V/ 3.6 V    |                 |                 | 4   | ms               |
| t <sub>CMErase</sub>        | Cumulative mass erase time                          | see Note 2            | 2.7 V/ 3.6 V    | 200             |                 |     | ms               |
|                             | Program/Erase endurance                             |                       |                 | 10 <sup>4</sup> | 10 <sup>5</sup> |     | cycles           |
| t <sub>Retention</sub>      | Data retention duration                             | T <sub>J</sub> = 25°C |                 | 100             |                 |     | years            |
| t <sub>Word</sub>           | Word or byte program time                           | see Note 3            |                 |                 | 35              |     | t <sub>FTG</sub> |
| t <sub>Block, 0</sub>       | Block program time for 1 <sup>st</sup> byte or word |                       |                 |                 | 30              |     |                  |
| t <sub>Block, 1-63</sub>    | Block program time for each additional byte or word |                       |                 |                 | 21              |     |                  |
| t <sub>Block, End</sub>     | Block program end-sequence wait time                |                       |                 |                 | 6               |     |                  |
| t <sub>Mass Erase</sub>     | Mass erase time                                     |                       |                 |                 | 5297            |     |                  |
| t <sub>Seg Erase</sub>      | Segment erase time                                  |                       |                 |                 | 4819            |     |                  |

- NOTES: 1. The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
2. The mass erase duration generated by the flash timing generator is at least 11.1ms ( = 5297x1/f<sub>FTG,max</sub> = 5297x1/476kHz). To achieve the required cumulative mass erase time the Flash Controller's mass erase operation can be repeated until this time is met. (A worst case minimum of 19 cycles are required).
3. These values are hardwired into the Flash Controller's state machine (t<sub>FTG</sub> = 1/f<sub>FTG</sub>).

## JTAG Interface

| PARAMETER             |                                       | TEST CONDITIONS | V <sub>CC</sub> | MIN | NOM | MAX | UNIT |
|-----------------------|---------------------------------------|-----------------|-----------------|-----|-----|-----|------|
| f <sub>TCK</sub>      | TCK input frequency                   | see Note 1      | 2.2 V           | 0   |     | 5   | MHz  |
|                       |                                       |                 | 3 V             | 0   |     | 10  | MHz  |
| R <sub>Internal</sub> | Internal pull-down resistance on TEST | see Note 2      | 2.2 V/ 3 V      | 25  | 60  | 90  | kΩ   |

- NOTES: 1. f<sub>TCK</sub> may be restricted to meet the timing requirements of the module selected.
2. TEST pull-down resistor implemented in all versions.

## JTAG Fuse (see Note 1)

| PARAMETER            |   | TEST CONDITIONS       | V <sub>CC</sub> | MIN | NOM | MAX | UNIT |
|----------------------|---|-----------------------|-----------------|-----|-----|-----|------|
| V <sub>CC</sub> (FB) | Supply voltage during fuse-blow condition     | T <sub>A</sub> = 25°C |                 | 2.5 |     |     | V    |
| V <sub>FB</sub>      | Voltage level on TEST for fuse-blow - 'C11x1  |                       |                 | 3.5 |     | 3.9 | V    |
|                      | Voltage level on TEST for fuse-blow - 'F11x1A |                       |                 | 6   |     | 7   | V    |
| I <sub>FB</sub>      | Supply current into TEST during fuse blow     |                       |                 |     |     | 100 | mA   |
| t <sub>FB</sub>      | Time to blow fuse                             |                       |                 |     |     | 1   | ms   |

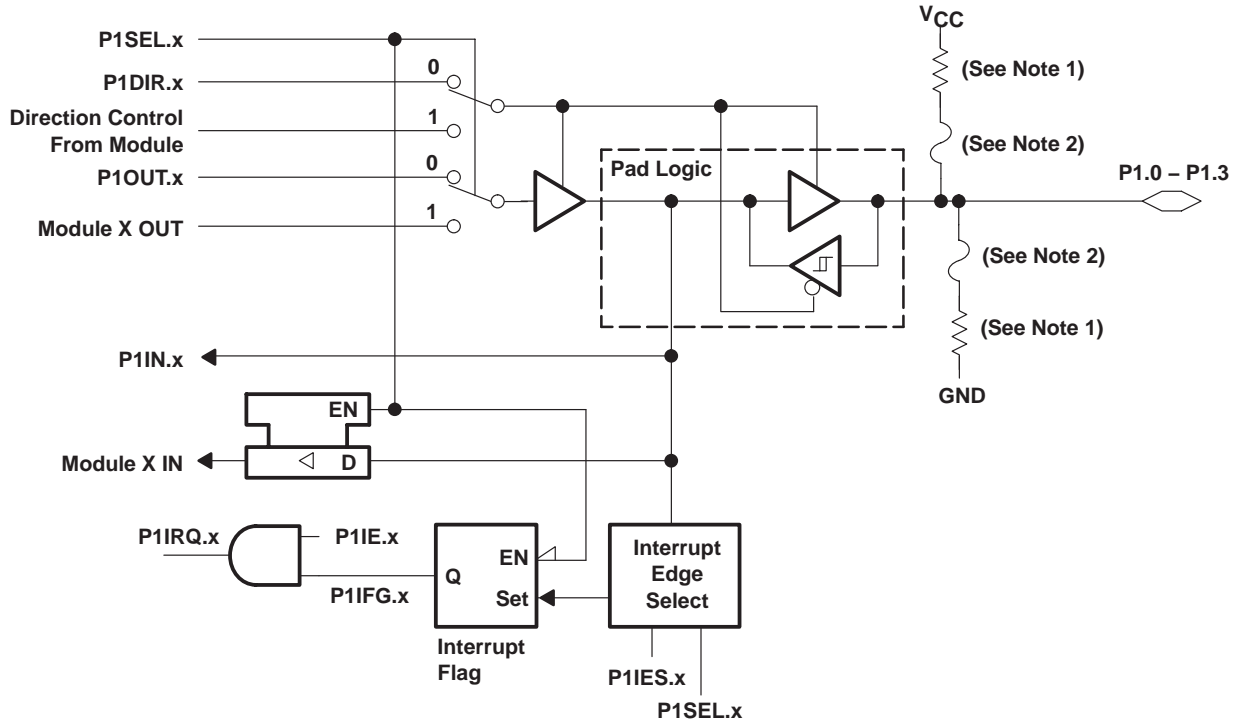
- NOTES: 1. Once the fuse is blown, no further access to the MSP430 JTAG/Test and emulation features is possible. The JTAG block is switched to bypass mode.



APPLICATION INFORMATION

input/output schematic

Port P1, P1.0 to P1.3, input/output with Schmitt-trigger



NOTE: x = Bit/identifier, 0 to 3 for port P1

| PnSel.x | PnDIR.x | Direction control from module | PnOUT.x | Module X OUT             | PnIN.x | Module X IN        | PnIE.x | PnIFG.x | PnIES.x |
|---------|---------|-------------------------------|---------|--------------------------|--------|--------------------|--------|---------|---------|
| P1Sel.0 | P1DIR.0 | P1DIR.0                       | P1OUT.0 | V <sub>SS</sub>          | P1IN.0 | TACLK <sup>†</sup> | P1IE.0 | P1IFG.0 | P1IES.0 |
| P1Sel.1 | P1DIR.1 | P1DIR.1                       | P1OUT.1 | Out0 signal <sup>†</sup> | P1IN.1 | CCI0A <sup>†</sup> | P1IE.1 | P1IFG.1 | P1IES.1 |
| P1Sel.2 | P1DIR.2 | P1DIR.2                       | P1OUT.2 | Out1 signal <sup>†</sup> | P1IN.2 | CCI1A <sup>†</sup> | P1IE.2 | P1IFG.2 | P1IES.2 |
| P1Sel.3 | P1DIR.3 | P1DIR.3                       | P1OUT.3 | Out2 signal <sup>†</sup> | P1IN.3 | CCI2A <sup>†</sup> | P1IE.3 | P1IFG.3 | P1IES.3 |

<sup>†</sup> Signal from or to Timer\_A

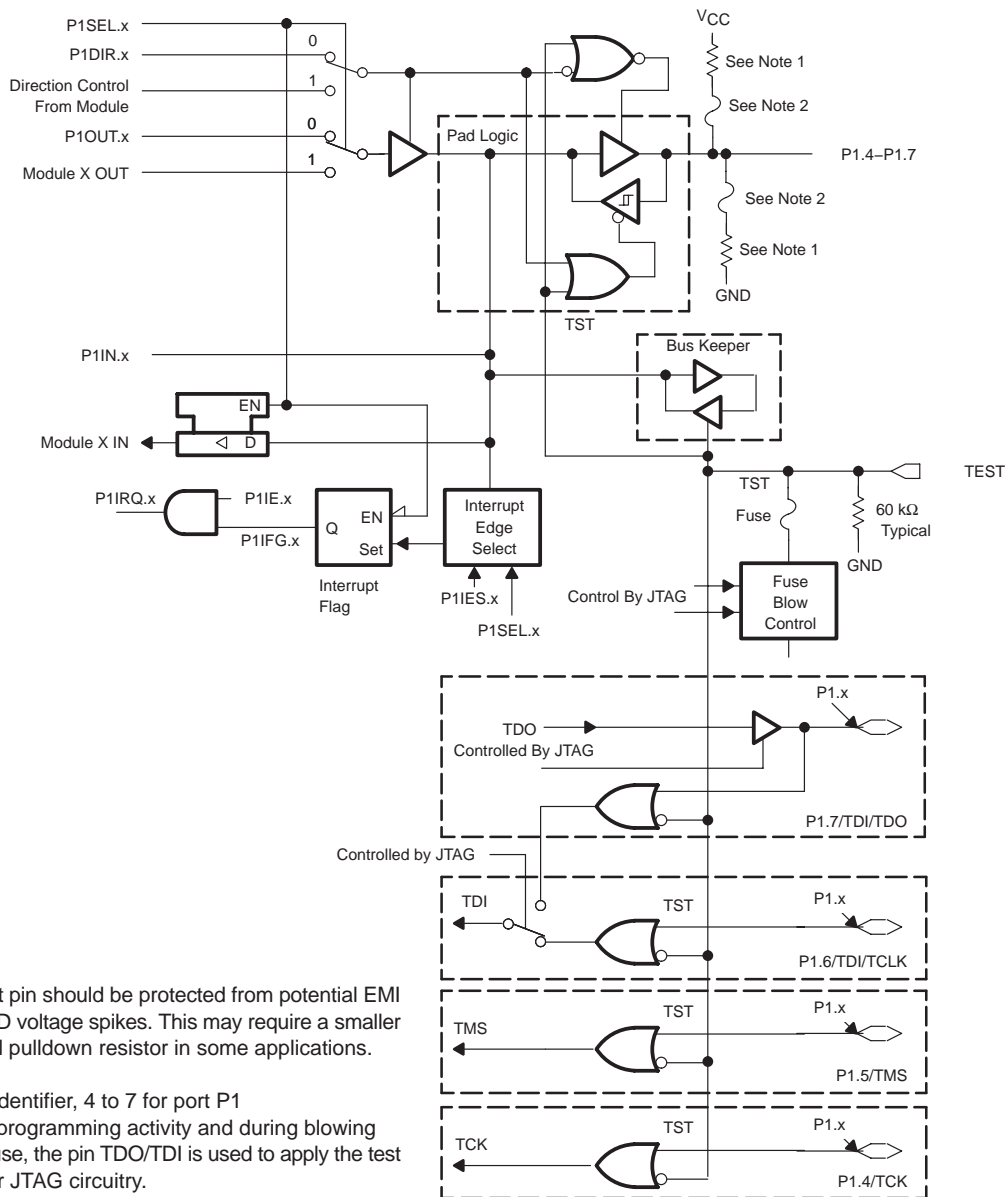
- NOTES: 1. Optional selection of pullup or pulldown resistors with ROM (masked) versions  
2. Fuses for optional pullup and pulldown resistors can only be programmed at the factory (ROM versions only).

# MSP430C11x1, MSP430F11x1A MIXED SIGNAL MICROCONTROLLER

SLAS241H – SEPTEMBER 1999 – REVISED SEPTEMBER 2004

## APPLICATION INFORMATION

### Port P1, P1.4 to P1.7, input/output with Schmitt-trigger and in-system access features



NOTE: The test pin should be protected from potential EMI and ESD voltage spikes. This may require a smaller external pulldown resistor in some applications.

x = Bit identifier, 4 to 7 for port P1

During programming activity and during blowing of the fuse, the pin TDO/TDI is used to apply the test input for JTAG circuitry.

| PnSel.x | PnDIR.x | Direction control from module | PnOUT.x | Module X OUT | PnIN.x | Module X IN | PnIE.x | PnIFG.x | PnIES.x |
|---------|---------|-------------------------------|---------|--------------|--------|-------------|--------|---------|---------|
| P1Sel.4 | P1DIR.4 | P1DIR.4                       | P1OUT.4 | SMCLK        | P1IN.4 | unused      | P1IE.4 | P1IFG.4 | P1IES.4 |
| P1Sel.5 | P1DIR.5 | P1DIR.5                       | P1OUT.5 | Out0 signal† | P1IN.5 | unused      | P1IE.5 | P1IFG.5 | P1IES.5 |
| P1Sel.6 | P1DIR.6 | P1DIR.6                       | P1OUT.6 | Out1 signal† | P1IN.6 | unused      | P1IE.6 | P1IFG.6 | P1IES.6 |
| P1Sel.7 | P1DIR.7 | P1DIR.7                       | P1OUT.7 | Out2 signal† | P1IN.7 | unused      | P1IE.7 | P1IFG.7 | P1IES.7 |

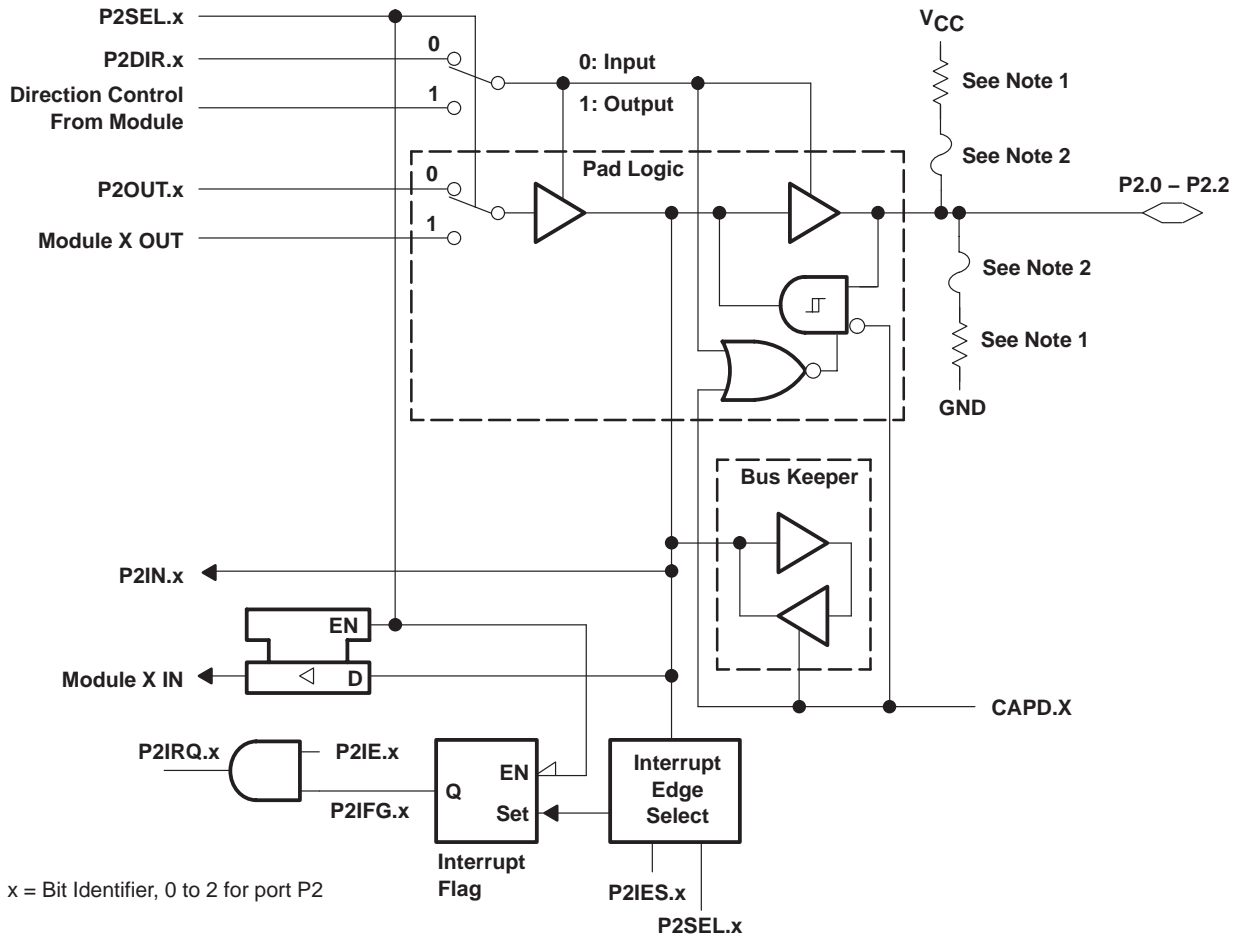
† Signal from or to Timer\_A

- NOTES: 1. Optional selection of pullup or pulldown resistors with ROM (masked) versions  
2. Fuses for optional pullup and pulldown resistors can only be programmed at the factory (ROM versions only).



APPLICATION INFORMATION

Port P2, P2.0 to P2.2, input/output with Schmitt-trigger



NOTE: x = Bit Identifier, 0 to 2 for port P2

| PnSel.x | PnDIR.x | Direction control from module | PnOUT.x | Module X OUT    | PnIN.x | Module X IN        | PnIE.x | PnIFG.x | PnIES.x |
|---------|---------|-------------------------------|---------|-----------------|--------|--------------------|--------|---------|---------|
| P2Sel.0 | P2DIR.0 | P2DIR.0                       | P2OUT.0 | ACLK            | P2IN.0 | unused             | P2IE.0 | P2IFG.0 | P1IES.0 |
| P2Sel.1 | P2DIR.1 | P2DIR.1                       | P2OUT.1 | V <sub>SS</sub> | P2IN.1 | INCLK <sup>†</sup> | P2IE.1 | P2IFG.1 | P1IES.1 |
| P2Sel.2 | P2DIR.2 | P2DIR.2                       | P2OUT.2 | CAOUT           | P2IN.2 | CCI0B <sup>†</sup> | P2IE.2 | P2IFG.2 | P1IES.2 |

<sup>†</sup> Signal from or to Timer\_A

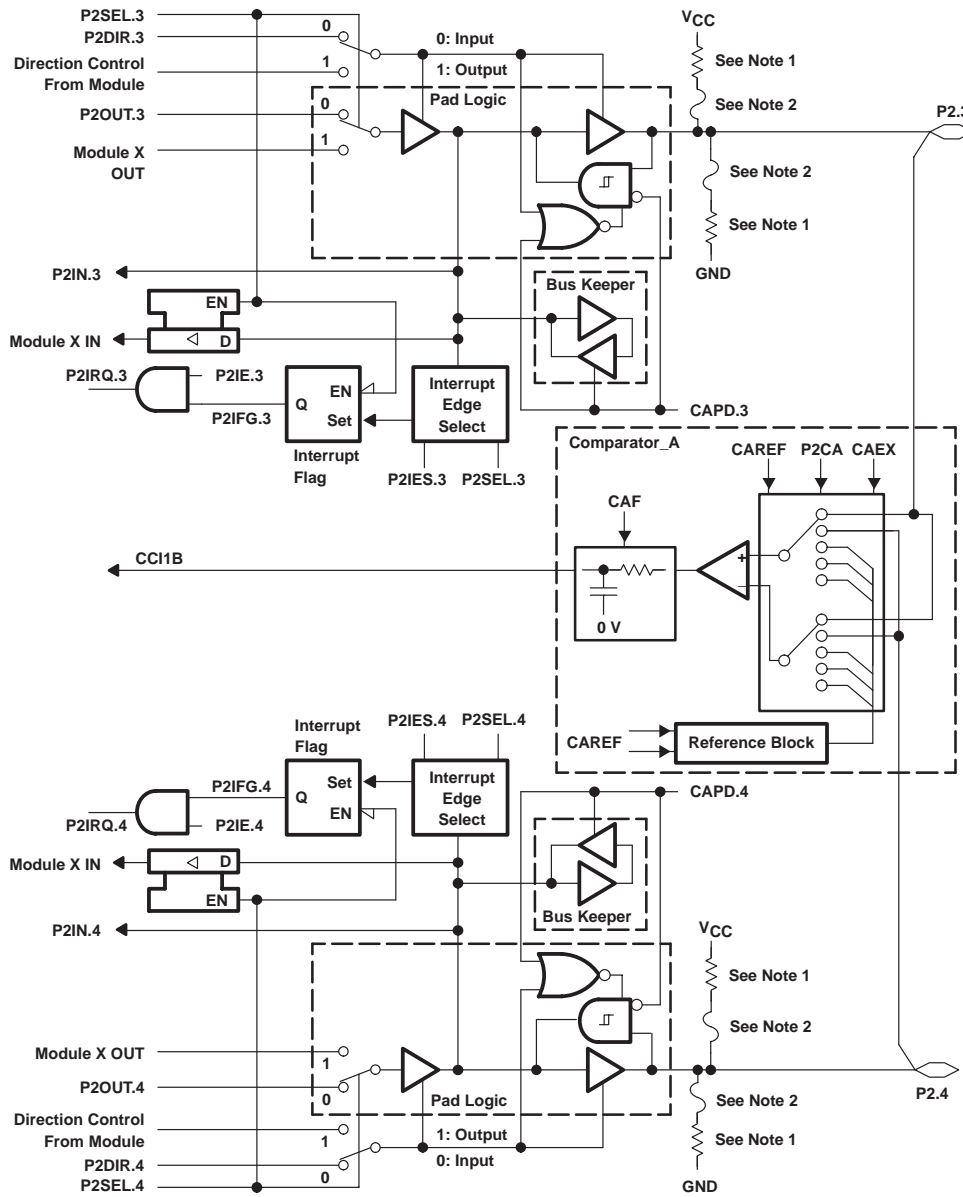
- NOTES: 1. Optional selection of pullup or pulldown resistors with ROM (masked) versions  
2. Fuses for optional pullup and pulldown resistors can only be programmed at the factory (ROM versions only).

# MSP430C11x1, MSP430F11x1A MIXED SIGNAL MICROCONTROLLER

SLAS241H – SEPTEMBER 1999 – REVISED SEPTEMBER 2004

## APPLICATION INFORMATION

### Port P2, P2.3 to P2.4, input/output with Schmitt-trigger



| PnSel.x | PnDIR.x | Direction control from module | PnOUT.x | Module X OUT             | PnIN.x | Module X IN | PnIE.x | PnIFG.x | PnIES.x |
|---------|---------|-------------------------------|---------|--------------------------|--------|-------------|--------|---------|---------|
| P2Sel.3 | P2DIR.3 | P2DIR.3                       | P2OUT.3 | Out1 signal <sup>†</sup> | P2IN.3 | unused      | P2IE.3 | P2IFG.3 | P1IES.3 |
| P2Sel.4 | P2DIR.4 | P2DIR.4                       | P2OUT.4 | Out2 signal <sup>†</sup> | P2IN.4 | unused      | P2IE.4 | P2IFG.4 | P1IES.4 |

<sup>†</sup> Signal from Timer\_A

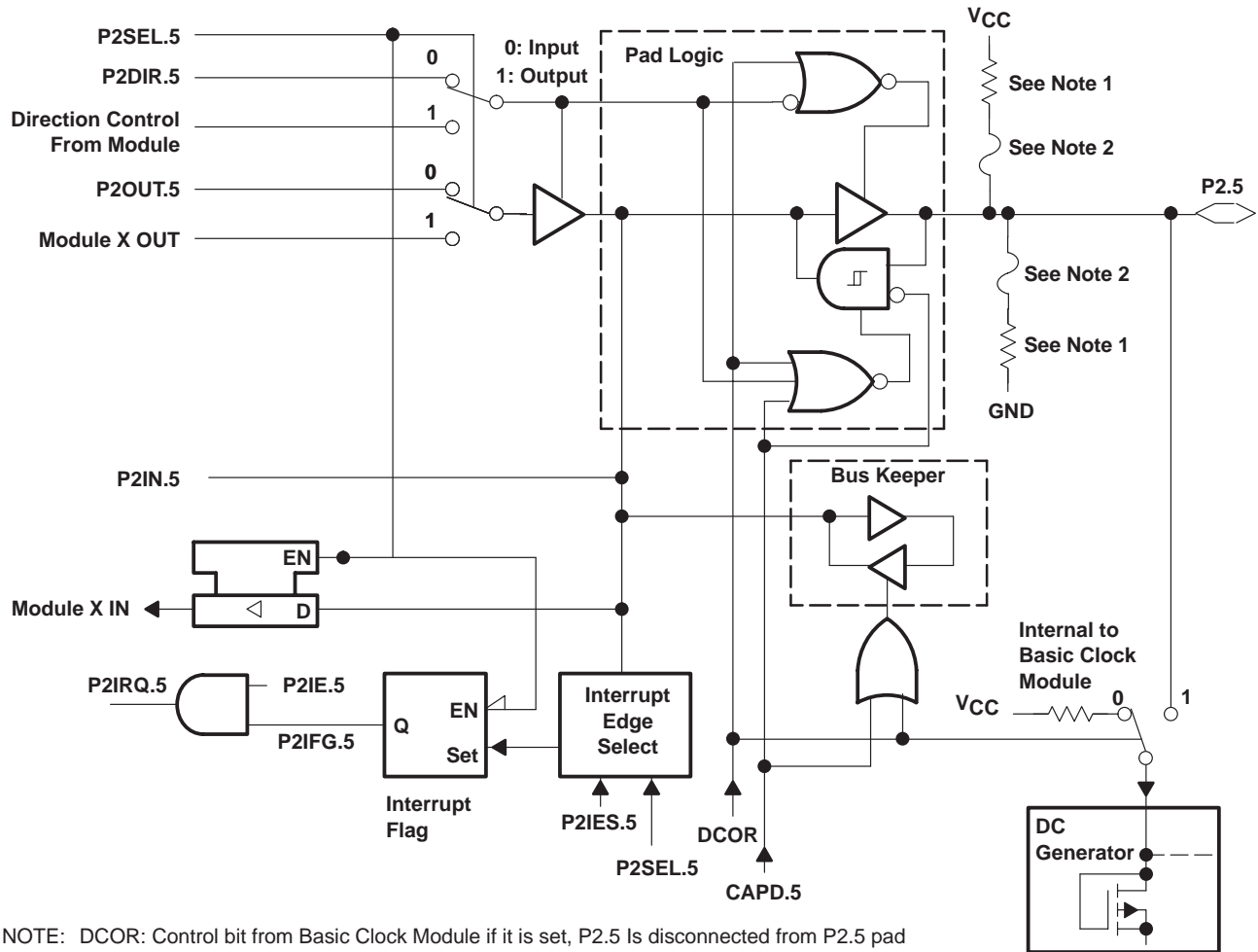
NOTES: 1. Optional selection of pullup or pulldown resistors with ROM (masked) versions  
2. Fuses for optional pullup and pulldown resistors can only be programmed at the factory (ROM versions only).



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APPLICATION INFORMATION

Port P2, P2.5, input/output with Schmitt-trigger and R<sub>OSC</sub> function for the Basic Clock module



NOTE: DCOR: Control bit from Basic Clock Module if it is set, P2.5 is disconnected from P2.5 pad

| PnSel.x | PnDIR.x | Direction control from module | PnOUT.x | Module X OUT    | PnIN.x | Module X IN | PnIE.x | PnIFG.x | PnIES.x |
|---------|---------|-------------------------------|---------|-----------------|--------|-------------|--------|---------|---------|
| P2Sel.5 | P2DIR.5 | P2DIR.5                       | P2OUT.5 | V <sub>SS</sub> | P2IN.5 | unused      | P2IE.5 | P2IFG.5 | P2IES.5 |

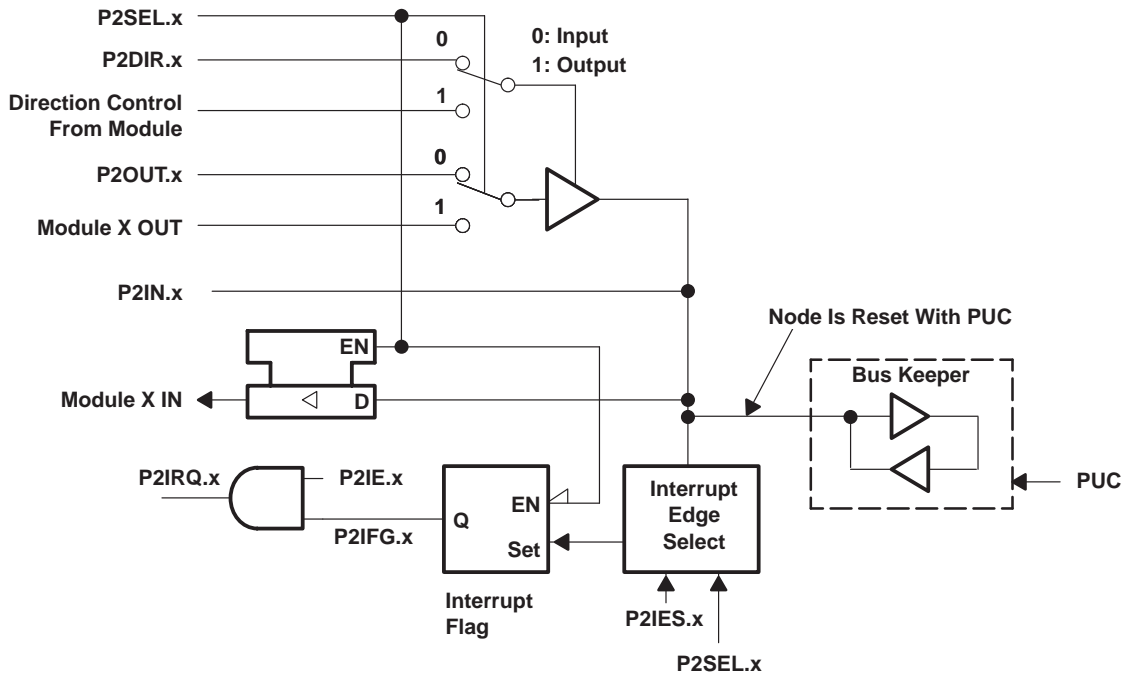
- NOTES: 1. Optional selection of pullup or pulldown resistors with ROM (masked) versions  
2. Fuses for optional pullup and pulldown resistors can only be programmed at the factory (ROM versions only).

# MSP430C11x1, MSP430F11x1A MIXED SIGNAL MICROCONTROLLER

SLAS241H – SEPTEMBER 1999 – REVISED SEPTEMBER 2004

## APPLICATION INFORMATION

### Port P2, unbonded bits P2.6 and P2.7



NOTE: x = Bit/identifier, 6 to 7 for port P2 without external pins

| P2Sel.x | P2DIR.x | Direction control from module | P2OUT.x | Module X OUT    | P2IN.x | Module X IN | P2IE.x | P2IFG.x | P2IES.x |
|---------|---------|-------------------------------|---------|-----------------|--------|-------------|--------|---------|---------|
| P2Sel.6 | P2DIR.6 | P2DIR.6                       | P2OUT.6 | V <sub>SS</sub> | P2IN.6 | unused      | P2IE.6 | P2IFG.6 | P2IES.6 |
| P2Sel.7 | P2DIR.7 | P2DIR.7                       | P2OUT.7 | V <sub>SS</sub> | P2IN.7 | unused      | P2IE.7 | P2IFG.7 | P2IES.7 |

NOTE 1: Unbonded bits 6 and 7 of port P2 can be used as software interrupt flags. The interrupt flags can only be influenced by software. They work then as a software interrupt.

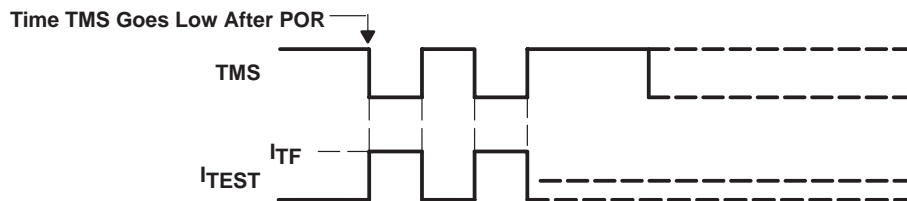
## JTAG fuse check mode

MSP430 devices that have the fuse on the TEST terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current,  $I_{TF}$ , of 1 mA at 3 V, 2.5 mA at 5 V can flow from the TEST pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

When the TEST pin is taken back low after a test or programming session, the fuse check mode and sense currents are terminated.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current will only flow when the fuse check mode is active and the TMS pin is in a low state (see Figure 13). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition).



**Figure 13. Fuse Check Mode Current, MSP430F11x1A and MSP430C11x1**

**NOTE:**

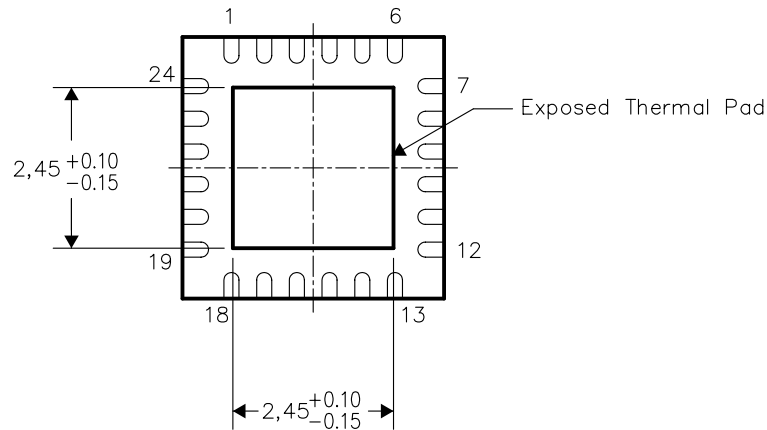
The CODE and RAM data protection is ensured if the JTAG fuse is blown and the 256-bit bootloader access key is used. Also, see the *bootstrap loader* section for more information.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

**PACKAGING INFORMATION**

| Orderable Device  | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|-------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| MSP430C1101       | ACTIVE                |              |                 |      |             | TBD                     | Call TI          | Call TI                      |
| MSP430F1101AIDGV  | ACTIVE                | TVSOP        | DGV             | 20   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| MSP430F1101AIDGVR | ACTIVE                | TVSOP        | DGV             | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| MSP430F1101AIDW   | ACTIVE                | SOIC         | DW              | 20   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| MSP430F1101AIDWR  | ACTIVE                | SOIC         | DW              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| MSP430F1101AIPW   | ACTIVE                | TSSOP        | PW              | 20   | 70          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| MSP430F1101AIPWR  | ACTIVE                | TSSOP        | PW              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| MSP430F1101AIRGER | ACTIVE                | QFN          | RGE             | 24   | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| MSP430F1101AIRGET | ACTIVE                | QFN          | RGE             | 24   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| MSP430F1111AIDGV  | ACTIVE                | TVSOP        | DGV             | 20   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| MSP430F1111AIDGVR | ACTIVE                | TVSOP        | DGV             | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| MSP430F1111AIDW   | ACTIVE                | SOIC         | DW              | 20   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| MSP430F1111AIDWR  | ACTIVE                | SOIC         | DW              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| MSP430F1111AIPW   | ACTIVE                | TSSOP        | PW              | 20   | 70          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| MSP430F1111AIPWR  | ACTIVE                | TSSOP        | PW              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| MSP430F1111AIRGER | ACTIVE                | QFN          | RGE             | 24   | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| MSP430F1111AIRGET | ACTIVE                | QFN          | RGE             | 24   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| MSP430F1121AIDGV  | ACTIVE                | TVSOP        | DGV             | 20   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| MSP430F1121AIDGVR | ACTIVE                | TVSOP        | DGV             | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| MSP430F1121AIDW   | ACTIVE                | SOIC         | DW              | 20   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| MSP430F1121AIDWR  | ACTIVE                | SOIC         | DW              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| MSP430F1121AIPW   | ACTIVE                | TSSOP        | PW              | 20   | 70          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| MSP430F1121AIPWR  | ACTIVE                | TSSOP        | PW              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| MSP430F1121AIRGER | ACTIVE                | QFN          | RGE             | 24   | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| MSP430F1121AIRGET | ACTIVE                | QFN          | RGE             | 24   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

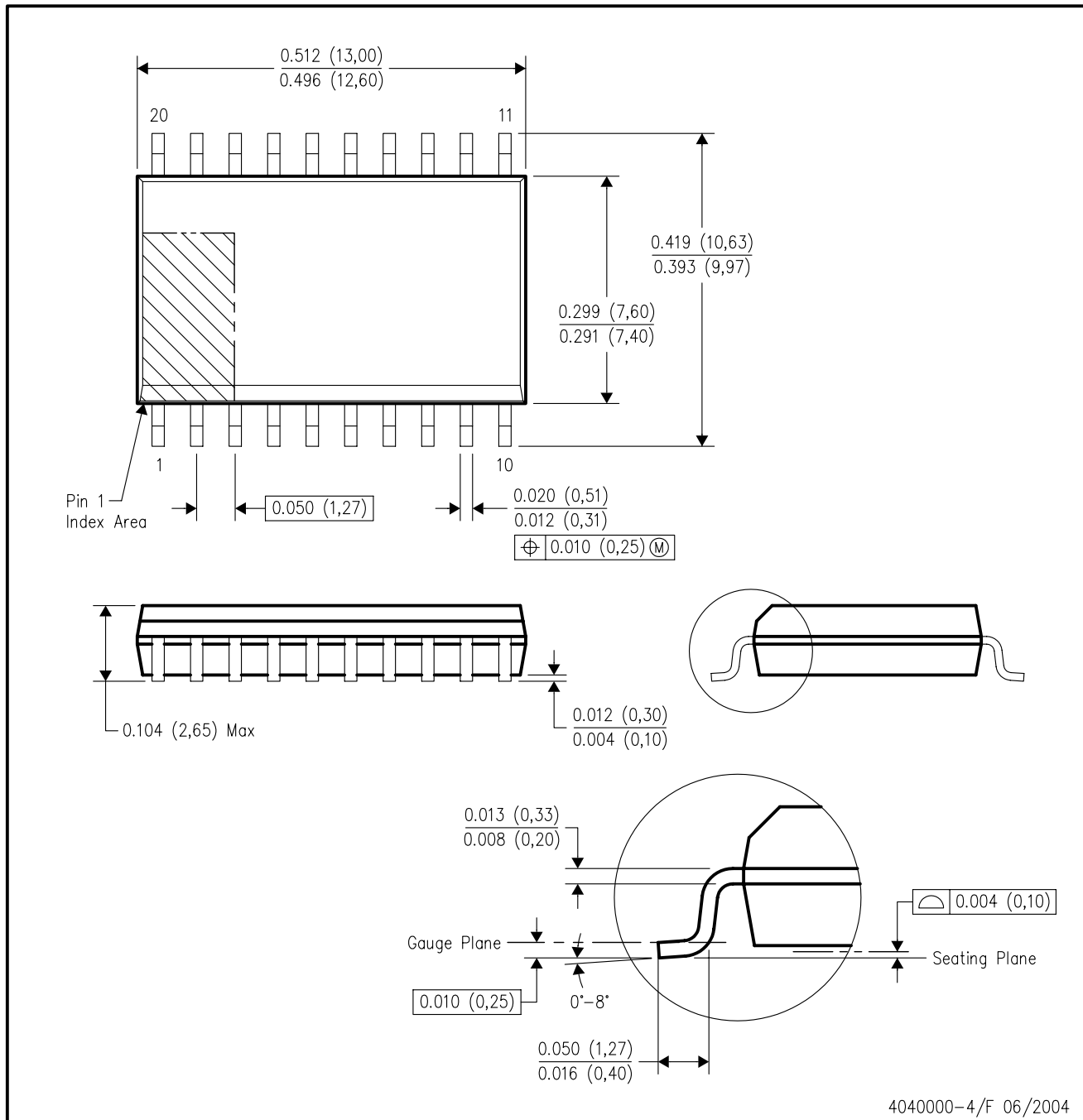


4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

DW (R-PDSO-G20)

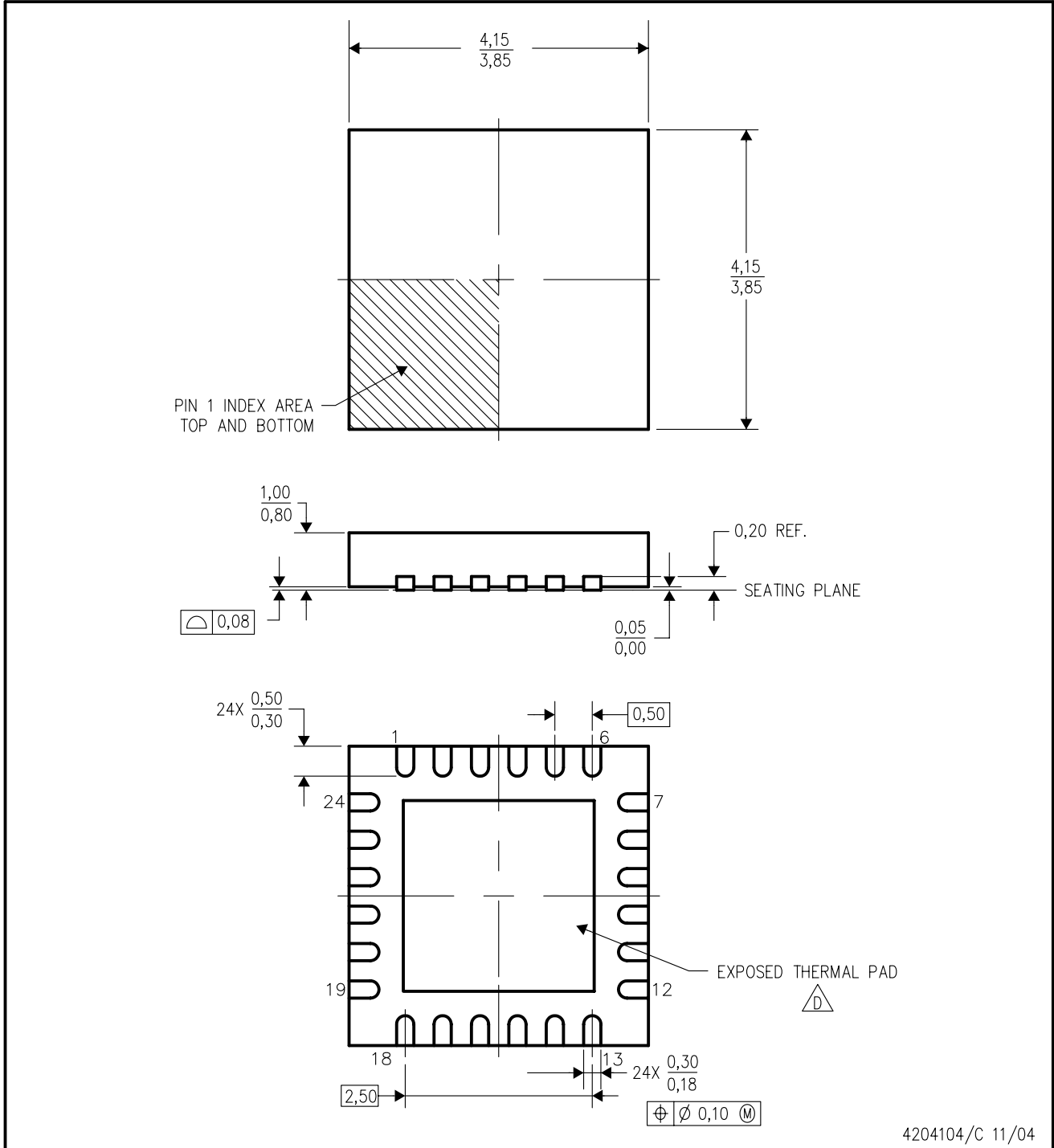
PLASTIC SMALL-OUTLINE PACKAGE




- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AC.

RGE (S-PQFP-N24)

PLASTIC QUAD FLATPACK



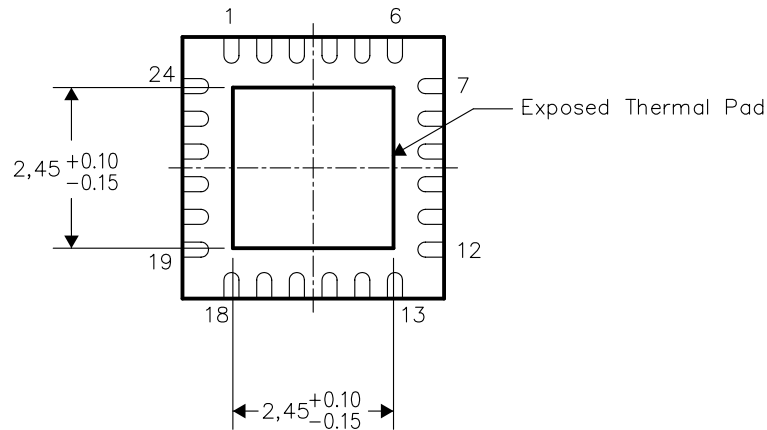
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Quad Flatpack, No-Leads (QFN) package configuration.
  -  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
  - E. Falls within JEDEC MO-220.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

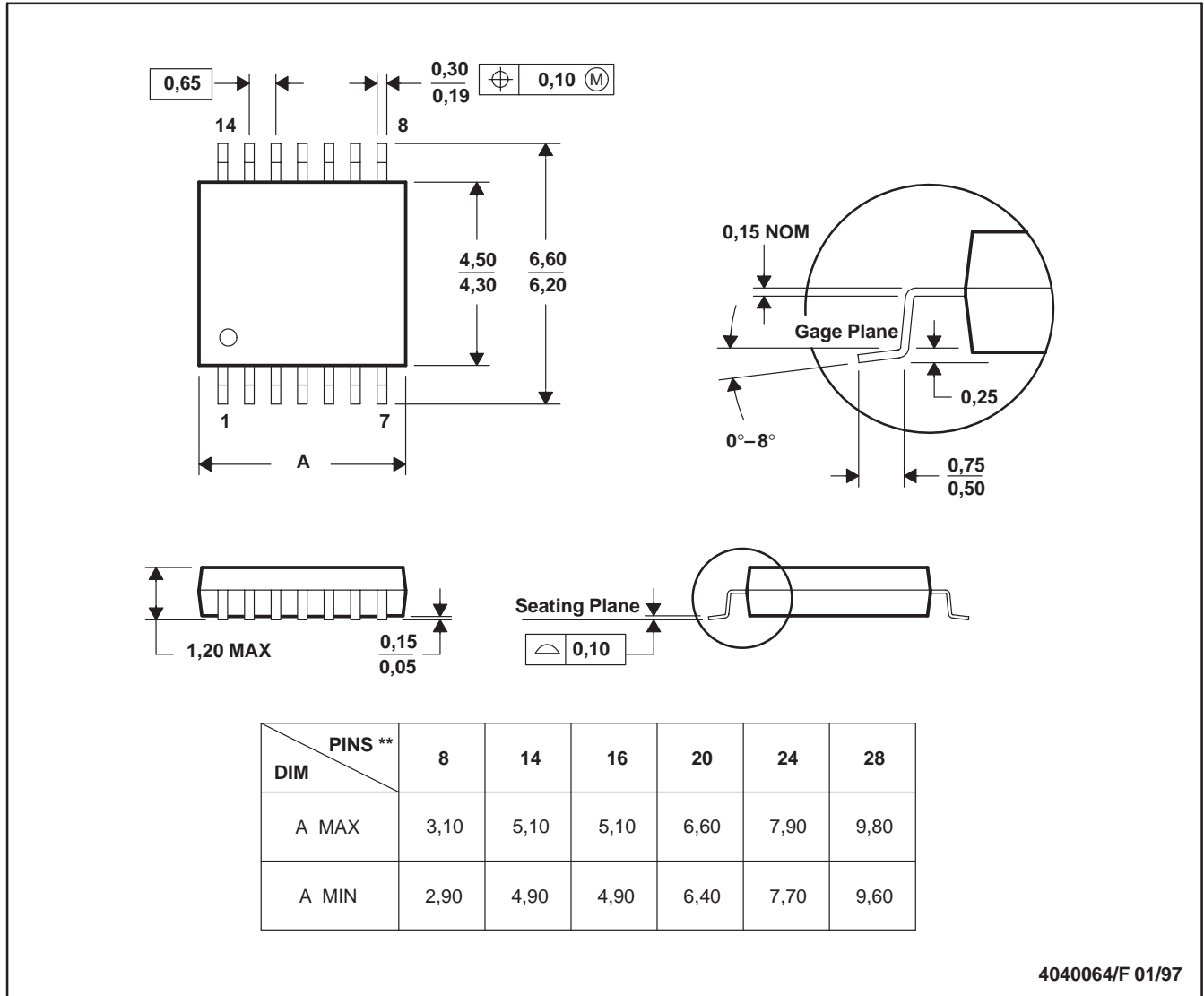
NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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