Patch (LVC75Z779 Eval Board Version 1E)

This document reports on a design mistake found on PCB layout of the LCD controller board (part # LVC75Z779 Eval Board Version 1E) and suggests a remedy for it.

Figure 1 shows an extract of the schematic. Pin 32 of SSD1928 is the PLL disable pin (PLL_DIS) for power down. The original design includes a 10k shunt to GND and this pin is wired to Pin 36 of JP1 for microcontroller.

A 0.1uF 0603 decoupling capacitor is required for this pin.

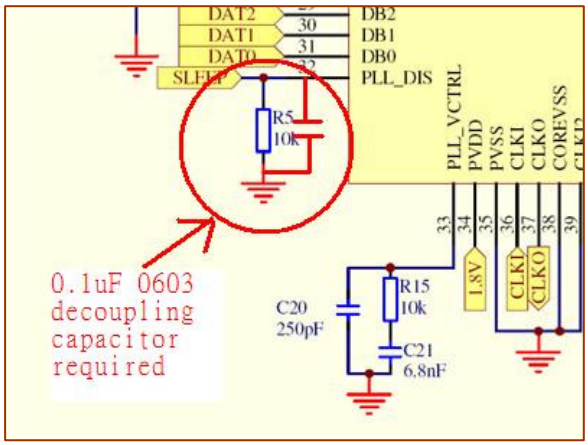

Figure 1 0.1uF 0603 decoupling cap required for pin 32

Please locate R5 on the component side as shown in Figure 2. Solder a 0.1uF 0603 ceramic capacitor on top of R5 (no R5 remove required). This action will greatly improve the stability.

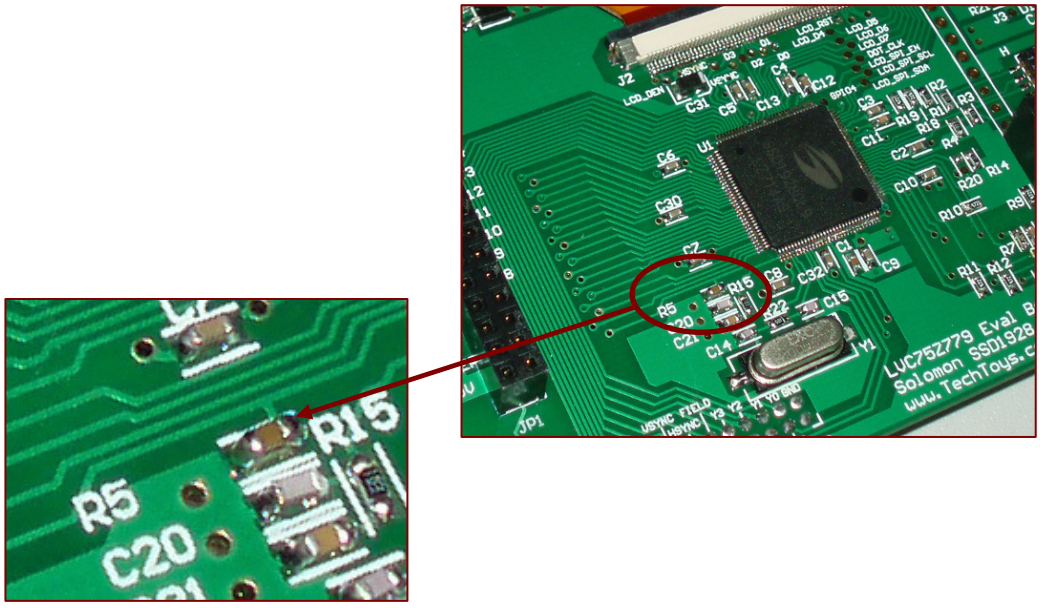

Figure 2 Solder a 0.1uF 0603 ceramic capacitor on top of R5 to improve stability

Boards shipped after 29th April 2009 will have this capacitor soldered prior to product shipment.