

Application Note

Device : S6B33B2B

132 RGB Segment & 162 Common Driver For 65,536 Color STN LCD

Jan. 11. 2004

Ver. 0.0

S6B33B2 Application Note Revision History		
Version	Content	Date
0.0	Initial Release	Jan. 2004

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1. INTRODUCTION

S6B33B2 is a mid-display-size-compatible driver for liquid crystal dot matrix gray-scale graphic systems. With on-chip CR oscillator circuit, the display-timing signal is generated without being sent from MPU. Also, it is capable of using 8bit/16bit data bus alternatively and operating with 68/80-series MPU in asynchronous. Due to the LCD driving signal (132 RGB X 162 output) corresponding to the display data and the internal bit-map display RAM of 132 X 163 X 16-bit, S6B33B2 is capable of operating max. 132 RGB X 162 dot LCD panels in low-power consumption.

Being the segment RGB 3-output, one pixel is 16-bit data and S6B33B2 can max display 65,536 color.

2. USE OF THE APPLICATION NOTE

This application note contains example of interconnecting panel and IC, of selecting passive elements and initializing program, etc. for regular operation of IC.

this document is guide book for LCD module engineers using this IC and hand set maker engineers using module mounting this IC.

3. FEATURES

3.1 Driver Output

- 132 RGB x 162

3.2 Gray Scale Function

Color depth	Red	Green	Blue
65,536	32 gray	64 gray	32 gray
4,096	16 gray	16 gray	16 gray
256	8 gray	8 gray	4 gray

3.3 On-chip Display Data RAM

- Capacity : 132 x 16 x 162 = 342.144k bits
- Burst RAM write function

3.4 Display Mode

- Normal display mode : Entire duty displaying
- Partial display mode : Partial duty displaying
- Area scroll mode : Particular area scrolling
- Standby mode : Internal display clocks off

3.5 Microprocessor Interface

- 8-bit/16 bit parallel bi-directional interface with 6800-series or 8080-series
- 3/4 Pin SPI (only write operation)

3.6 On-chip Low Power Analog Circuit

- On-chip CR oscillator (Internal cap. & external resistor), external clock available
- Voltage converter / Voltage regulator / Voltage follower
- On-chip electronic contrast control (256 steps)

3.7 Operating Voltage Range

- VDD : 1.8 ~ 3.3V (Without Internal Regulator)
2.4 ~ 3.3V (With internal Regulator)
- VIN1 : 2.4 ~ 3.6V
- Display operating voltage(V1) : 2.0 ~ 4.0V
- LCD Operating Voltage Range : Max. 20V

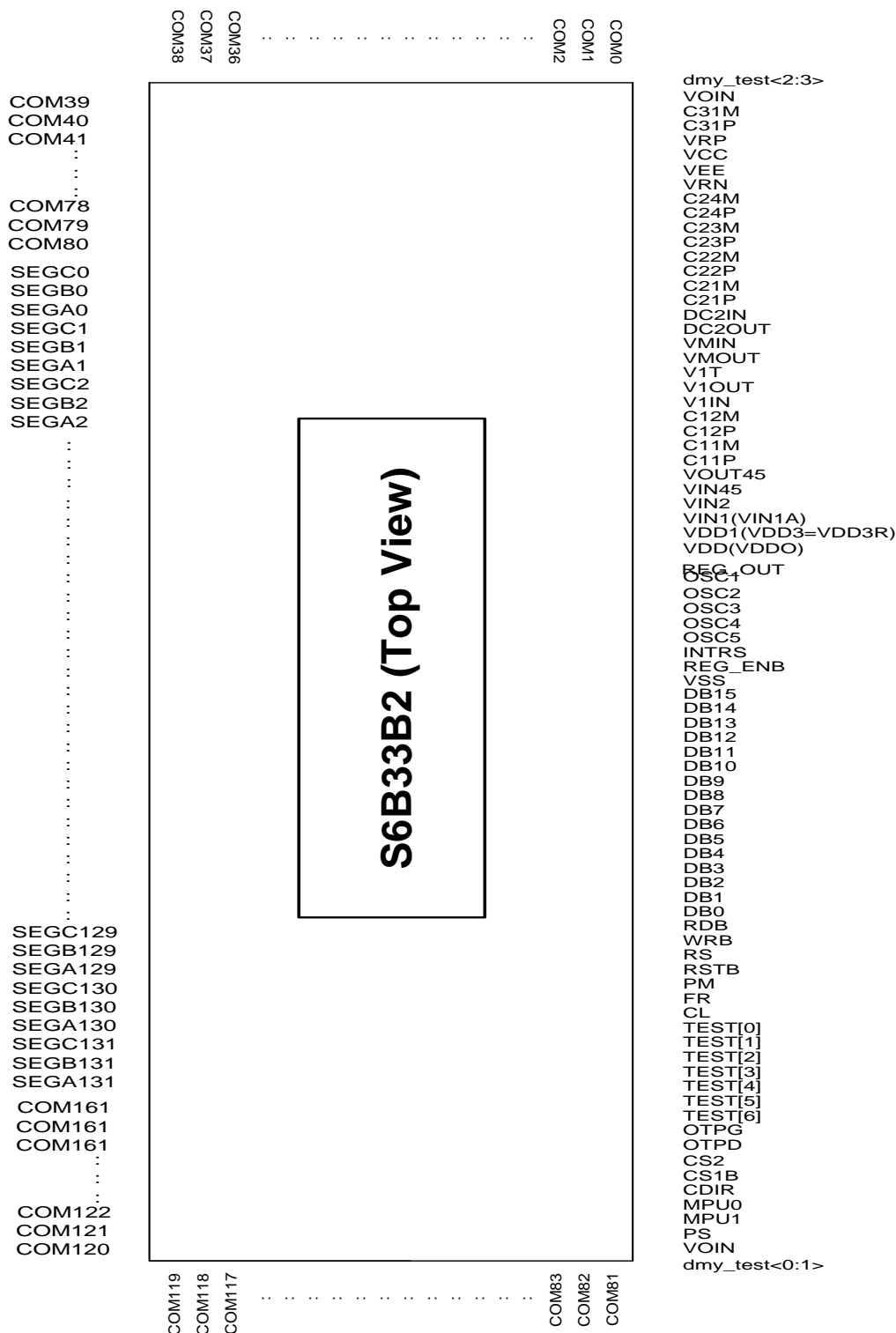
3.8 Package Type

- COG (Output Pad Pitch Min. 40 μm)

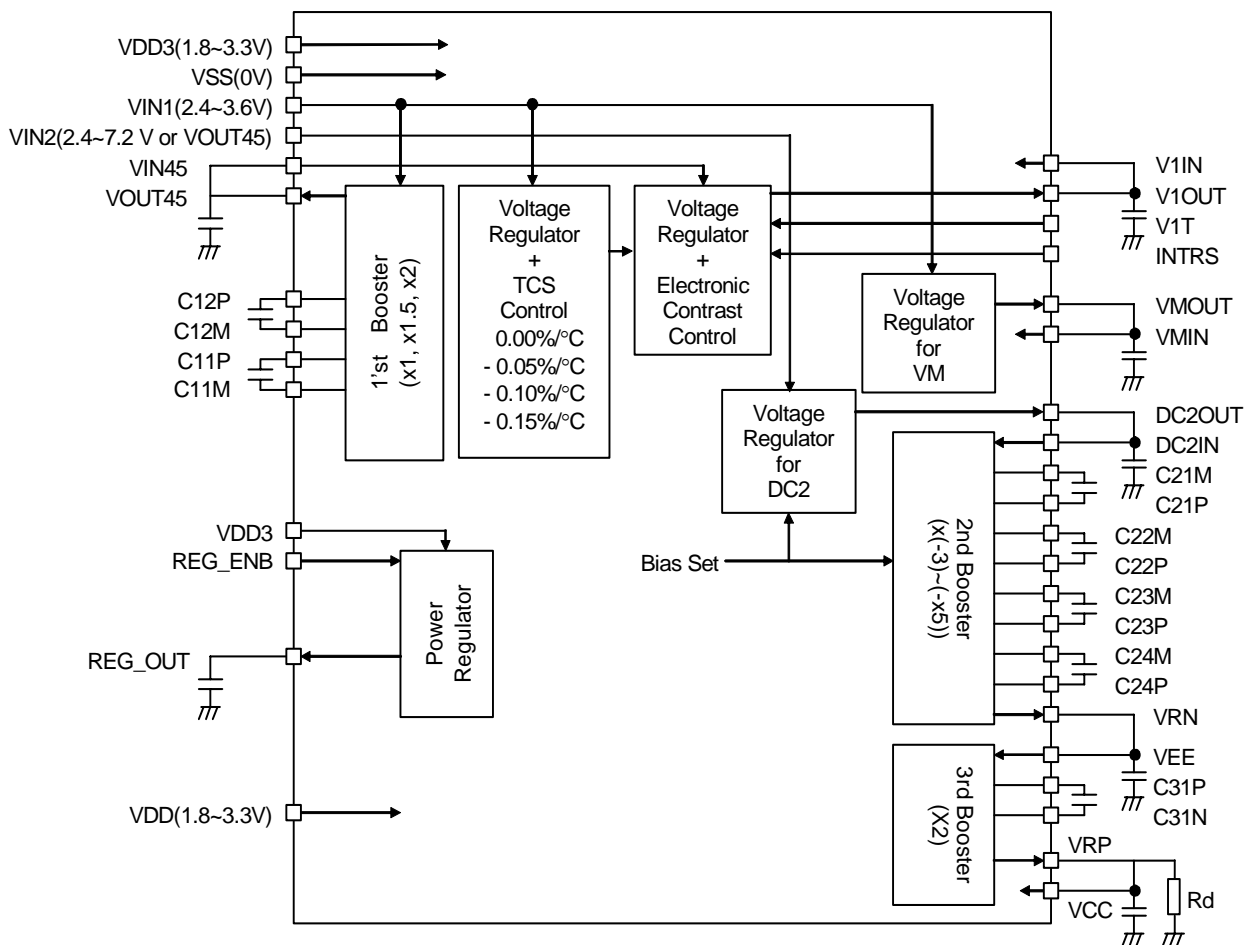
3.9 Special Features

- Non-Volatile Memory for V1 Calibration

4. PIN CONFIGURATION



5. POWER BLOCK DIAGRAM



6. CALCULATION OF EACH VOLTAGE LEVEL

The Calculation of LCD driving Voltage for S6B33B2

$V_{ev} = (1 - (255 -) / 512) \times 2.0$, here = 0~255 value of contrast control register.

$V1 = 2 \times V_{ev}$, @V1OUT terminal

$VM = V1/2$ @VMOUT terminal

$DC2 = 3/4 \times V1$ (when 1/4 bias) @DC2OUT Terminal

= $4/6 \times V1$ (When 1/5 bias)

= $5/6 \times V1$ (When 1/6 bias)

= $6/8 \times V1$ (When 1/7 bias)

$VEE = DC2 \times (-2)$ (When 1/4 bias) @VSS level

= $DC2 \times (-3)$ (When 1/5 bias) @VSS level

= $DC2 \times (-3)$ (When 1/6 bias) @VSS level

= $DC2 \times (-4)$ (When 1/7 bias) @VSS level

$VCC = -(VEE) + V1$

7. SUPPLY VOLTAGE RANGE

7.1 1'st Booster Setting

- * VIN1 : Input voltage of the 1'st booster circuit
Power source of the voltage regulator for Vref and TCS circuit
Power source of the voltage regulator for VMOUT
- * VIN2 : Power source of the voltage regulator for DC2OUT
- * VOUT45 : Power source of the voltage regulator for V1OUT and
Electronic contrast control circuit

Once the maximum V1 value of module is decided from Vop of LCD panel (using Equation 6), determine the setting value of 1'st booster, referencing below table according to VIN1 voltage value.

At this time, below condition must be satisfied.

VOUT45 - V1OUT > 0.5V (in case of using 1'st booster)

or VOUT45 - V1OUT > 0.3V (in case of using external power)

Unit : Volt

VIN1	1'st booster setting	VOUT45	Available range of V1
2.4	X 1.5	3.6	2.0~3.1
	X 2.0	4.8	2.0~4.0
2.7	X 1.0	2.7	2.0~2.2
	X 1.5	4.05	2.0~3.55
	X 2.0	5.4	2.0~4.0
3.0	X 1.0	3.0	2.0~2.5
	X 1.5	4.5	2.0~4.0
	X 2.0	6.0	2.0~4.0
3.3	X 1.0	3.3	2.0~2.8
	X 1.5	4.95	2.0~4.0
	X 2.0	6.6	2.0~4.0
3.6	X 1.0	3.6	2.0~3.1
	X 1.5	5.4	2.0~4.0
	X 2.0	7.2	2.0~4.0

- * Because above VOUT45 output values come from theoretically calculation when 1'st Booster circuit is on, real output value may be a little lower depending on the environment such as Panel load and cap. value etc.

(Red color : Recommend value)

7.2 VIN2=VOUT45

(Recommended)

Unit : Volt

VIN1	1'st booster setting value	VOUT45	DC2OUT (V1X5/6, V1=2~4V)
2.4	X 1.0	2.4	1.67~1.9
	X 1.5	3.6	1.67~3.1
	X 2.0	4.8	1.67~3.3
2.7	X 1.0	2.7	1.67~2.2
	X 1.5	4.05	1.67~3.3
	X 2.0	5.4	1.67~3.3
3.0	X 1.0	3.0	1.67~2.5
	X 1.5	4.5	1.67~3.3
	X 2.0	6.0	1.67~3.3
3.3	X 1.0	3.3	1.67~2.8
	X 1.5	4.95	1.67~3.3
	X 2.0	6.6	1.67~3.3
3.6	X 1.0	3.6	1.67~3.1
	X 1.5	5.4	1.67~3.3
	X 2.0	7.2	1.67~3.3

* If you connect VIN2 to VDD3, you must consider below.

When you supply 3.3V(maximum voltage of VDD3) to VDD3, DC2OUT can be up to 3.3V as normal case and there is no effect on display characteristic.

But when supplying 3V, maximum output voltage of DC2OUT cannot be over 3V and it is impossible to control contrast up to the higher voltage than 3V.

So, we recommend to connect VIN2 to VOUT45 according to the proper value at the table listed above except when supplying 3.3V to VDD3.

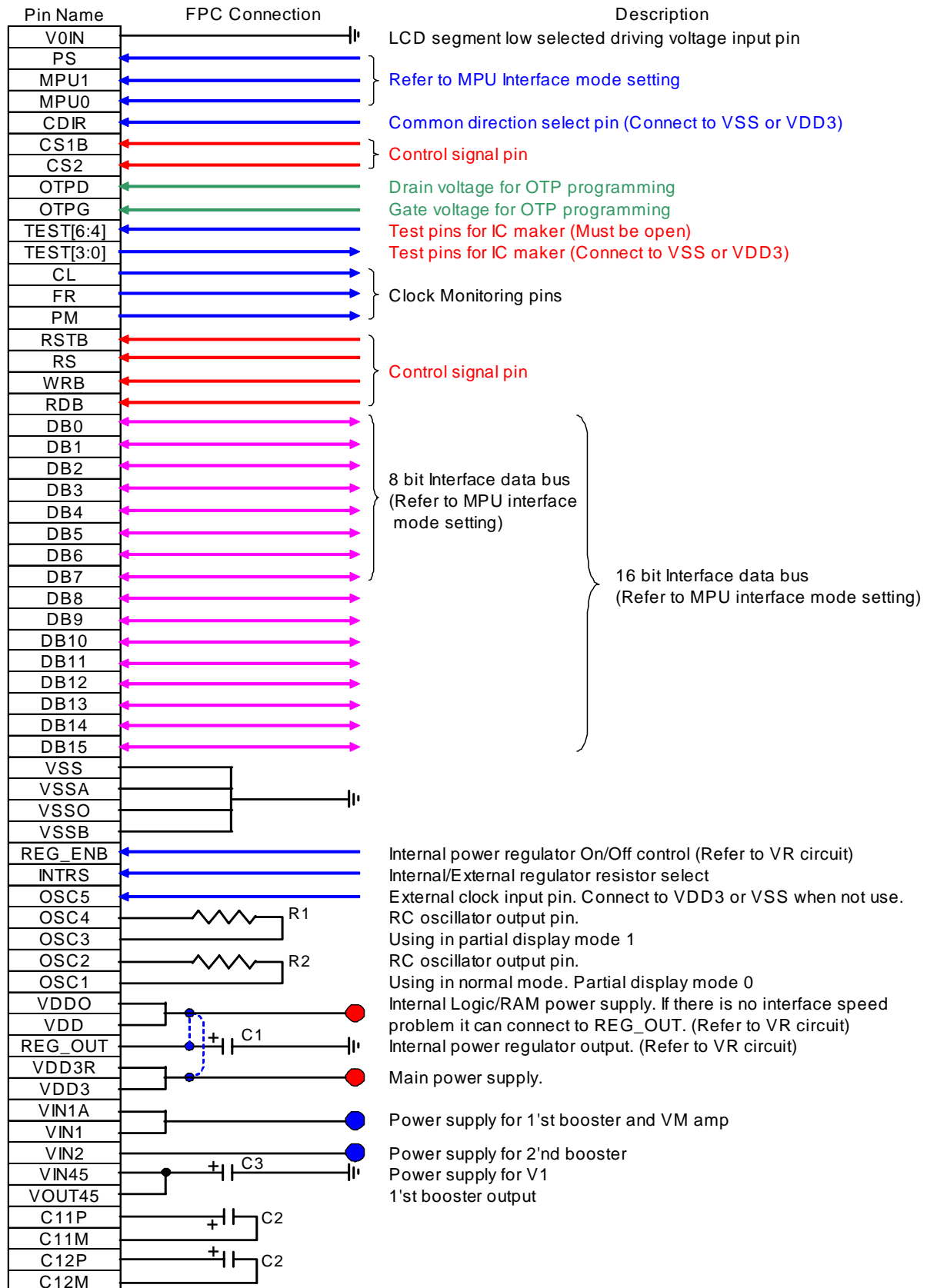
At this time, below condition must be satisfied.

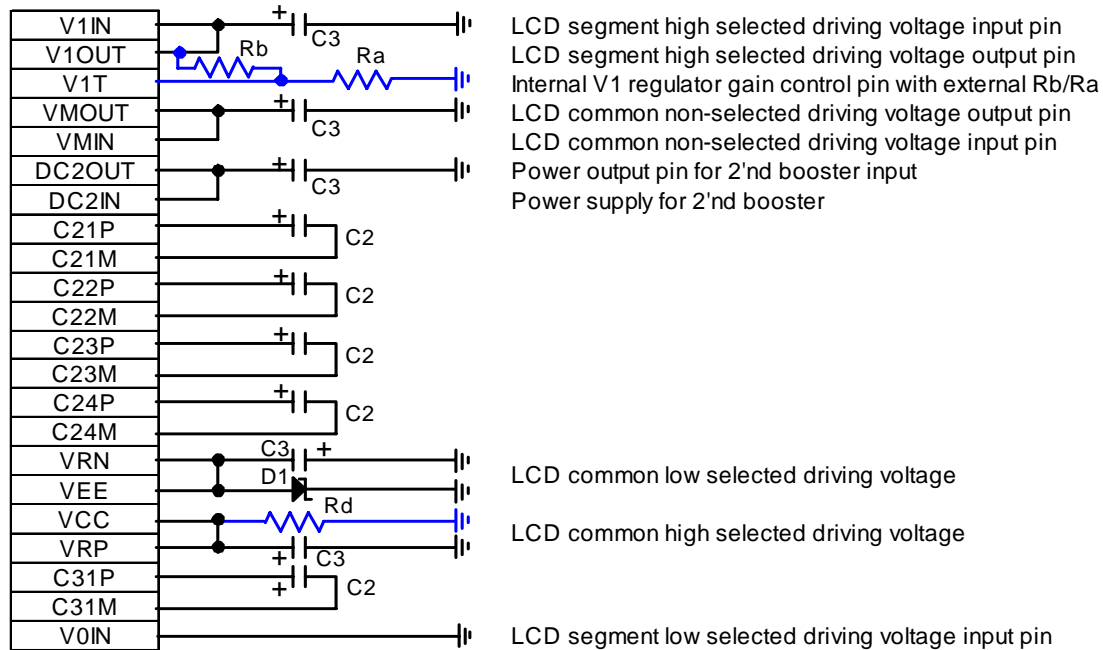
VIN2 - DC2OUT > 0.5V (in case of using 1'st booster)

or VIN2 - DC2OUT > 0.3V (in case of using External power)

On the other hand, if VDD3 ranges from 2.4V to 3.3V, it is general to connect VIN1 to VDD3 and set the 1'st booster properly.

8. INTERCONNECTION CIRCUIT SCHEMATIC





9. OPTIONAL CAPACITORS & RESISTORS VALUE

9.1 Values of External Components

Item	Device	Value
C1	Capacitor	1.0 to 4.7F
C2	Capacitor	1.0 to 2.2F
C3	Capacitor	1.0 to 2.2F
D1	Schottky barrier diode	Vforward = Max. 0.3V at 1mA Vreverse = Min. 15V
Rd	Discharge Resistor	Typ. 1M ohm

9.2 Maximum Rating Voltage of Capacitors

Item	Maximum Rating Voltage	Item	Maximum Rating Voltage
REG_OUT to VSS	3V	C21P to C21M	5V
VOUT45 to VSS	11V	C22P to C22M	10V
C11P to C11M	6V	C23P to C23M	13V
C12P to C12M	6V	C24P to C24M	13V
VMOUT to VSS	3V	VSS to VRN	13V
DC2OUT to VSS	5V	C31P to C31M	17V
V1OUT to VSS	6V	VRP to VSS	18V

10. MPU INTERFACE MODE SETTING

10.1 Parallel Interface (PS="H")

MPU[1]	MPU[0]	CS1B	CS2	RDB	WRB	Data Bus	MPU Type
L	L	CS1B	CS2	RDB	WRB	DB[7:0]	8080 Series
	H	CS1B	CS2			DB[15:0]	
H	L	CS1B	CS2	E	R/W	DB[7:0]	6800 Series
	H	CS1B	CS2			DB[15:0]	

* MPU[1] : Select the MPU type

* MPU[0] : Select the mode of data bus

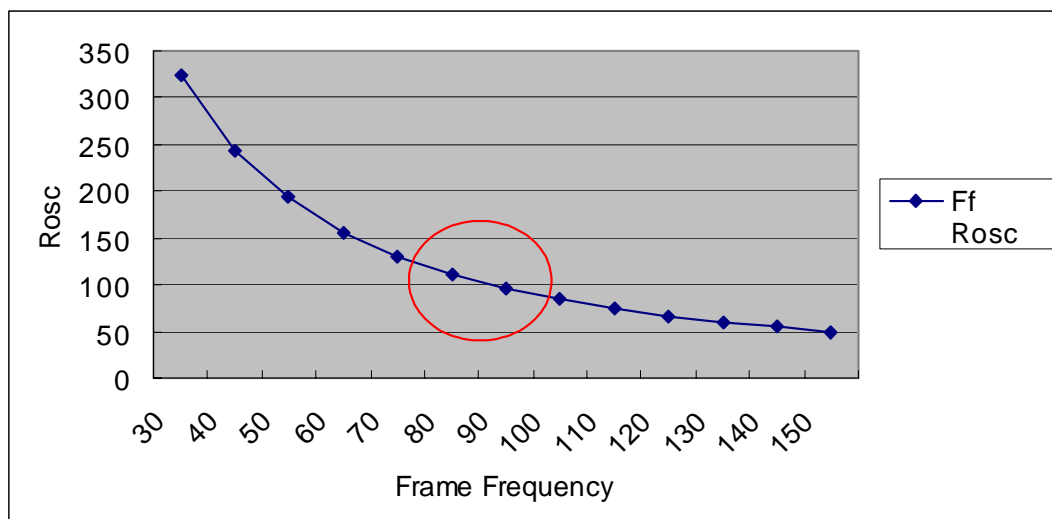
* In accessing internal registers (D/I = "L"), only DB[7:0] are valid.

10.2 Serial Interface(PS="L")

PS	MPU[1]	CS1B	CS2	D/I	Serial Data	Serial Mode	SPI Mode
L	L	CS1B	CS2	By S/W	DB[7]	DB[6]	3 pin
	H	CS1B	CS2	D/I			4 pin

* Read operations are not allowed.

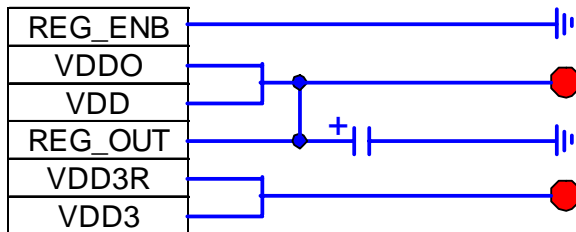
11. RELATION BETWEEN OSC. RESISTOR & FREQUENCY



* Above graph shows real measured values using the 128 x 160 dots STN LCD module mounting S6B33B2. (VDD3=VIN1=2.8V, VIN2=VOUT45, 1/5bias, 1/162duty)
Red circle : Recommend value.

12. VOLTAGE REGULATOR MODE SETTING

12.1 Type “A” : Using Internal Regulator Circuit

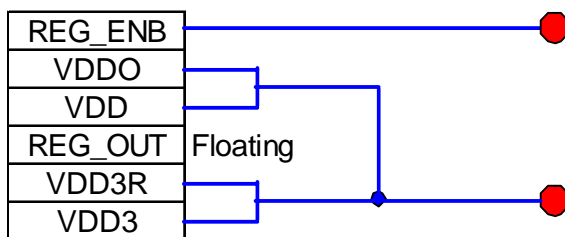


VDD3 : 2.4 to 3.3V

REG_OUT : 2.0V(Typ)

Merit : Power consumption is smaller than type “B”

12.2 Type “B” : Non Using Internal Regulator Circuit



VDD3 : 1.8 to 3.3V

Merit : Memory write cycle is faster than type “A”

13. RECOMMENDED ITO RESISTANCE VALUE

Function	Pin Name	ITO Resistance
System power	VDD3, VDD3R, VDD, VSS, VSSO, VSSA, VSSB, REG_OUT, OTPD	20
Driver power	V1IN, VMIN, V0IN, VCC, VEE V1OUT, VMOUT, VRP, VRN	50
Boosting power	VIN1, VIN1A, VIN2, VIN45, VOUT45 DC2IN, DC2OUT	50
Boosting cap.	C11+/-, C12+/-, C21+/-, C22+/-, C23+/- C24+/-, C31+/-	50
Oscillator	OSC1, OSC2, OSC3, OSC4, OSC5	100
System control	RSTB, PS, MPU1/2, CDIR, INTRS, REG_ENB	300
MPU interface	CS1B, CS2, D/I(RS), WRB(R/W), RD(E), DB[15:0]	300
Others	V1T	300

14. CONSIDERATIONS FOR ESD

It is not allowed to connect dummy pads to any part of an ITO line.

Dummy pad must be left open. Because they do not have ESD protection circuit.

15. POWER ON/OFF SEQUENCE

15.1 Power On

Standby Off OSC On 1'st Booster On Wait 20mS AMP On
Wait 20mS 2'nd Booster On Wait 20mS 3'rd Booster On
Wait 20mS Display On

15.2 Power Off

Standby On (delay over 20ms) VDD3 off

15.3 Power Recover

Standby On Standby Off Display On

16. S6B33B2 GRAY SCALE

Method	R	G	B
PWM	8	8	8
FRC	4	8	4
Possible Gray Level	32	64	32

17. SOFTWARE EXAMPLE

* Module Condition

128 RGB X 160 dots, 65K color mode, 8080 mode 16bit I/F, VDD3 = VIN1 = 3.0V
VIN2 = VOUT45, 1'st and 2'nd Booster = 1.5 times, TCS = 0.00%/1/162 duty, 1/5 bias, Red/Blue output swap

```
#define OSCILLATION_MODE_SET    0x02
#define DRIVER_OUTPUT_MODE_SET  0x10
#define DC_DC_SET               0x20
#define CURRENT_BIAS_SET        0x22
#define PCK_GENER_MODE_SET      0x24 // = DCDC Clock division set
#define DCDC_AMP_ON_OFF_SET     0x26
#define TEMP_COMPENSATION_SET   0x28
#define CONTRAST_CONTROL1       0x2A
#define CONTRAST_CONTROL2       0x2B
#define STANDBY_MODE_OFF        0x2C
#define STANDBY_MODE_ON         0x2D
#define DDRAM_BURST_MODE_OFF    0x2E
#define DDRAM_BURST_MODE_ON     0x2F
#define ADDRESSING_MODE_SET     0x30
#define ROW_VECTOR_MODE_SET     0x32
#define N_LINE_INVERSION_SET    0x34 // = N-Block Inversion
#define FRAME_FREQUENCY_CONTROL_SET 0x36
#define ENTRY_MODE_SET          0x40
#define X_ADDRESS_AREA_SET      0x42
#define Y_ADDRESS_AREA_SET      0x43
#define RAM_SKIP_AREA_SET       0x45
#define DISPLAY_OFF             0x50
#define DISPLAY_ON              0x51
#define SPEC_DISPLAY_PATTERN_SET 0x53
#define PARTIAL_DISPLAY_MODE_SET 0x55
#define PARTIAL_DISPLAY_START_LINE_SET 0x56
#define PARTIAL_DISPLAY_END_LINE_SET 0x57
#define AREA_SCROLL_MODE_SET    0x59
#define SCROLL_START_LINE_SET   0x5A
#define SET_DISPLAY_DATA_LENGTH 0xFC
```

// Standby mode off

```
outpw(HS_LCD_INDEX_REG, STANDBY_MODE_OFF);
```

```
// Select internal or external OSC clock and OSC On/Off control
outpw(HS_LCD_INDEX_REG, OSCILLATION_MODE_SET);
outpw(HS_LCD_INDEX_REG, 0x01); // Use internal OSC and OSC On

// Select the first booster's boosting step for V1 generation
outpw(HS_LCD_INDEX_REG, DC_DC_SET);
outpw(HS_LCD_INDEX_REG, 0x05); // X1.5 step for normal mode(with partial mode 0)
                                and partial mode 1

// Control the 1'st booster, V1 AMP, 2'nd booster and 3'rd booster
outpw(HS_LCD_INDEX_REG, DCDC_AMP_ON_OFF_SET);
outpw(HS_LCD_INDEX_REG, 0x01); // 1'st booster On

clk_long_busy_wait(20000); // Waiting 20mS for 1'st booster output stabilization

outpw(HS_LCD_INDEX_REG, DCDC_AMP_ON_OFF_SET);
outpw(HS_LCD_INDEX_REG, 0x09); // 1'st booster and V1 AMP On

clk_long_busy_wait(20000); // Waiting 20mS for V1 AMP output stabilization

outpw(HS_LCD_INDEX_REG, DCDC_AMP_ON_OFF_SET);
outpw(HS_LCD_INDEX_REG, 0x0B); // 1'st booster, V1 AMP and 2'nd booster On

clk_long_busy_wait(20000); // Waiting 20mS for 2'nd booster output stabilization

outpw(HS_LCD_INDEX_REG, DCDC_AMP_ON_OFF_SET);
outpw(HS_LCD_INDEX_REG, 0x0F); // 1'st booster, V1 AMP, 2'nd booster and
                                3'rd booster On

clk_long_busy_wait(20000); // Waiting 20mS for 3'rd booster output stabilization

// Set the temperature compensation ratio
outpw(HS_LCD_INDEX_REG, TEMP_COMPENSATION_SET);
outpw(HS_LCD_INDEX_REG, 0x00); // 0.00 % /

// Burst mode off for data RAM write
outpw(HS_LCD_INDEX_REG, DDRAM_BURST_MODE_OFF);
// when burst mode on, data RAM write data length change to 32bit regardless MPU
interface setting.
```



```
// RAM address skip area setting
outpw(HS_LCD_INDEX_REG, RAM_SKIP_AREA_SET);
outpw(HS_LCD_INDEX_REG, 0x00); // Set to No skip
//outpw(HS_LCD_INDEX_REG, 0x02); // 3ch-47h skip

// Specified display pattern select
outpw(HS_LCD_INDEX_REG, SPEC_DISPLAY_PATTERN_SET);
outpw(HS_LCD_INDEX_REG, 0x00); // Normal display.
// outpw(HS_LCD_INDEX_REG, 0x01); // Reverse display.
// outpw(HS_LCD_INDEX_REG, 0x02); // All display off
// outpw(HS_LCD_INDEX_REG, 0x03); // All display on

// Select number of display line, Segment direction and Red/Blue output swap
outpw(HS_LCD_INDEX_REG, DRIVER_OUTPUT_MODE_SET);
outpw(HS_LCD_INDEX_REG, 0x22); // 1/162 duty and Red/Blue output swap

// DCDC Clock division set
outpw(HS_LCD_INDEX_REG, PCK_GENER_MODE_SET);
outpw(HS_LCD_INDEX_REG, 0x11); // fosc/8 division for normal(with partial mode 0)
                                and partial mode 1

// Addressing mode set
outpw(HS_LCD_INDEX_REG, ADDRESSING_MODE_SET);
outpw(HS_LCD_INDEX_REG, 0x1C); // 65K color mode, Dummy sub group off,
                                sub group frame inversion on,
                                sub group inversion off,
                                sub group phase change every 2 pixel unit.

// Row vector mode set
outpw(HS_LCD_INDEX_REG, ROW_VECTOR_MODE_SET);
outpw(HS_LCD_INDEX_REG, 0x0E); // Row vector increment period : Every sub-frame
                                Row vector sequence : R1 R2 R3 R4 R1...

// Entry mode set
outpw(HS_LCD_INDEX_REG, ENTRY_MODE_SET);
outpw(HS_LCD_INDEX_REG, 0x00); // Non-Reverse, Y-direction prefer, Read modify off

// Y-address area set(for segment direction)
outpw(HS_LCD_INDEX_REG, Y_ADDRESS_AREA_SET);
outpw(HS_LCD_INDEX_REG, 0x00); // from 0
```

```
outpw(HS_LCD_INDEX_REG, 0x7F); // to 127 for 128 segment
```

```
// X-address area set(for common direction)
```

```
outpw(HS_LCD_INDEX_REG, X_ADDRESS_AREA_SET);
```

```
outpw(HS_LCD_INDEX_REG, 0x00); // from 0
```

```
outpw(HS_LCD_INDEX_REG, 0x9F); // to 159 for 160 common
```

```
// N-line inversion set
```

```
outpw(HS_LCD_INDEX_REG, N_LINE_INVERSION_SET);
```

```
outpw(HS_LCD_INDEX_REG, 0x0D); // FIM=off, FIP=off, N-BLK=13
```

```
// Frame frequency control
```

```
outpw(HS_LCD_INDEX_REG, FRAME_FREQUENCY_CONTROL_SET);
```

```
outpw(HS_LCD_INDEX_REG, 0x00); // Low frequency set off
```

```
// Contrast control for partial display mode 1
```

```
outpw(HS_LCD_INDEX_REG, CONTRAST_CONTROL2);
```

```
outpw(HS_LCD_INDEX_REG, 0x20); // Can be change for suitable contrast
```

```
// Contrast control for normal display and partial display mode 0
```

```
outpw(HS_LCD_INDEX_REG, CONTRAST_CONTROL1);
```

```
outpw(HS_LCD_INDEX_REG, 0xBF); // Can be change for suitable contrast
```

```
// Driving current and bias set
```

```
outpw(HS_LCD_INDEX_REG, CURRENT_BIAS_SET);
```

```
outpw(HS_LCD_INDEX_REG, 0x11); // Normal current driving mode and 1/5 bias for  
                                all display mode
```

```
// Partial display mode set
```

```
outpw(HS_LCD_INDEX_REG, PARTIAL_DISPLAY_MODE_SET);
```

```
outpw(HS_LCD_INDEX_REG, 0x00); // Partial display mode off
```

```
// Display start line set for all partial display mode
```

```
outpw(HS_LCD_INDEX_REG, PARTIAL_DISPLAY_START_LINE_SET);
```

```
outpw(HS_LCD_INDEX_REG, 0x00);
```

```
// Display end line set for all partial display mode
```

```
outpw(HS_LCD_INDEX_REG, PARTIAL_DISPLAY_END_LINE_SET);
```

```
outpw(HS_LCD_INDEX_REG, 0x9F);
```

```
// Area scroll set
```

```
outpw(HS_LCD_INDEX_REG, AREA_SCROLL_MODE_SET);
```

```
outpw(HS_LCD_INDEX_REG, 0x00); // Area scroll mode off(Entire display)
```

```
outpw(HS_LCD_INDEX_REG, 0x00); // Scroll area start line
```

```
outpw(HS_LCD_INDEX_REG, 0x9F); // Scroll area end line
```

```
outpw(HS_LCD_INDEX_REG, 0x00); // Lower fixed number
```

```
// Scroll start line set when use area scroll set
```

```
outpw(HS_LCD_INDEX_REG, SCROLL_START_LINE_SET);
```

```
outpw(HS_LCD_INDEX_REG, 0x00);
```

```
// Write initial display data
```

```
outpw(HS_LCD_CTRL_REG, lcd_init_image[128*i+j]);
```

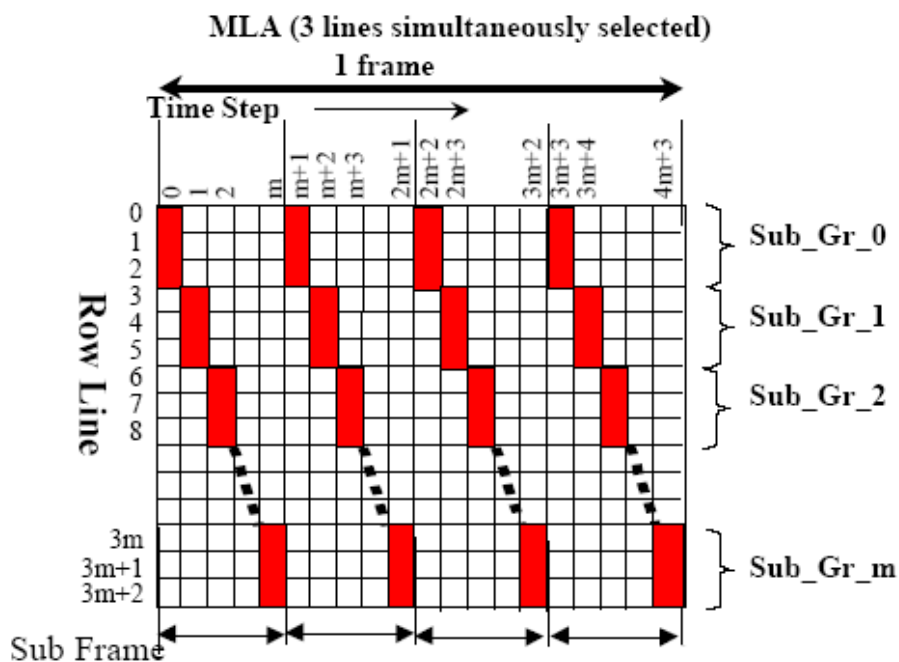
```
//Display On
```

```
outpw(HS_LCD_INDEX_REG, DISPLAY_ON);
```

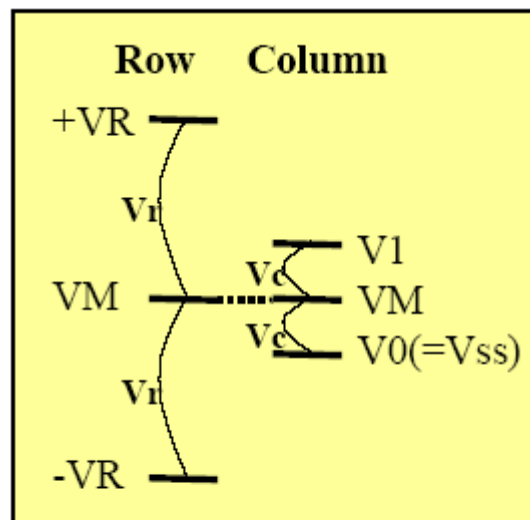
18. 3LINE MLA DRIVING METHOD

18.1 Scanning Sequence of MLA

- * 3 lines are selected simultaneously
- * MLA equally distributed type



18.2 Definition of Driving Voltages



- Selected (+VR or -VR applied)
- Non-selected (VM applied)

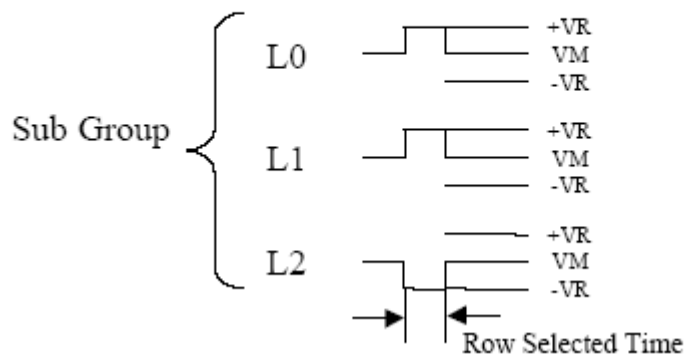
18.3 Generation of Row Function & Row Wave Form

- * The polarity of voltage (+VR, -VR) of the selected row lines is determined by row function.
- * Row voltage is determined by the column of 3 X 4 row function matrix.
- * 3 X 4 Row function

	R1	R2	R3	R4
L0	0	1	1	1
L1	1	0	1	1
L2	1	1	0	1

note) 1 represents +VR, 0 represents -VR

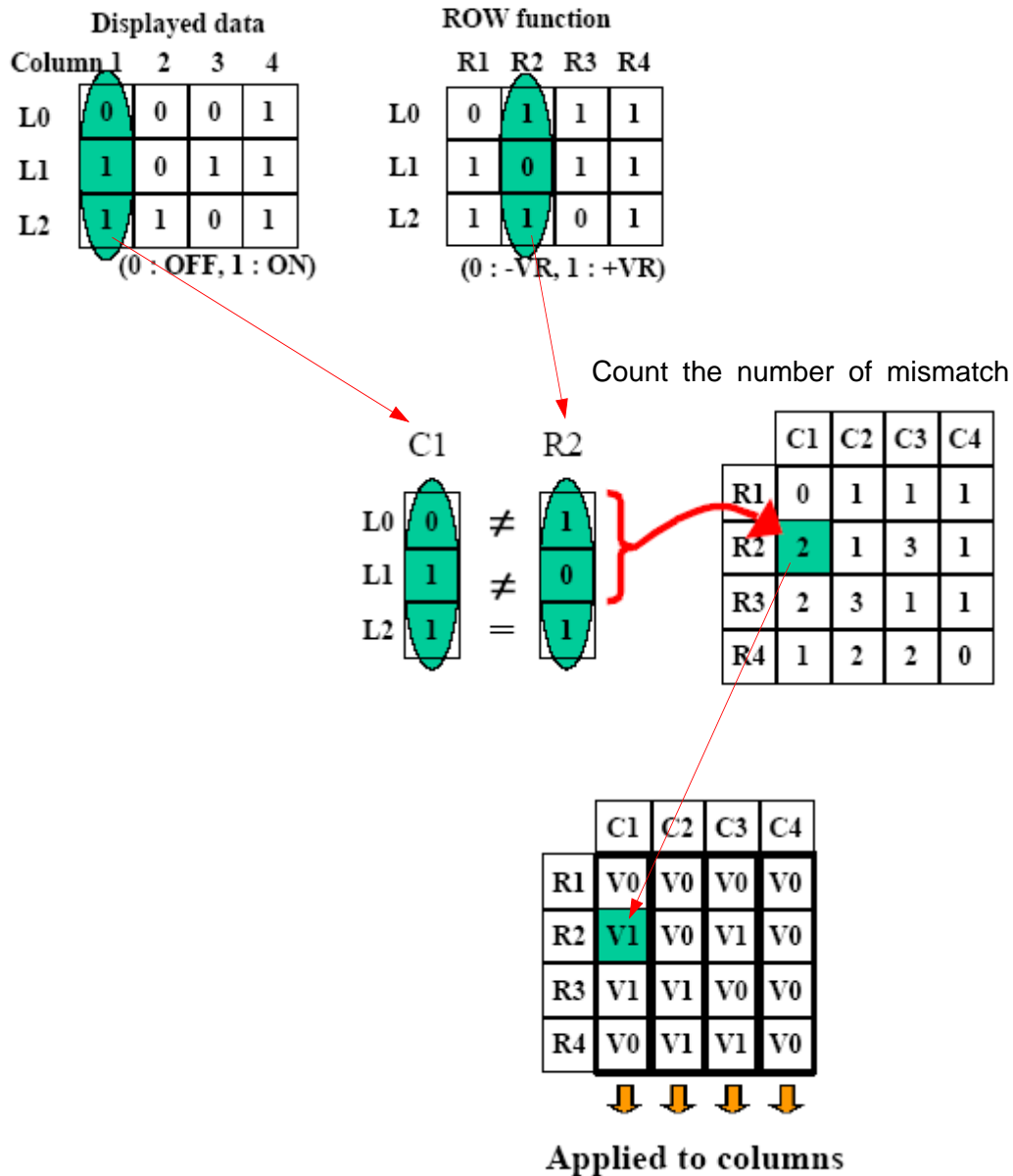
Row output waveform at the case when R3 vector is selected.

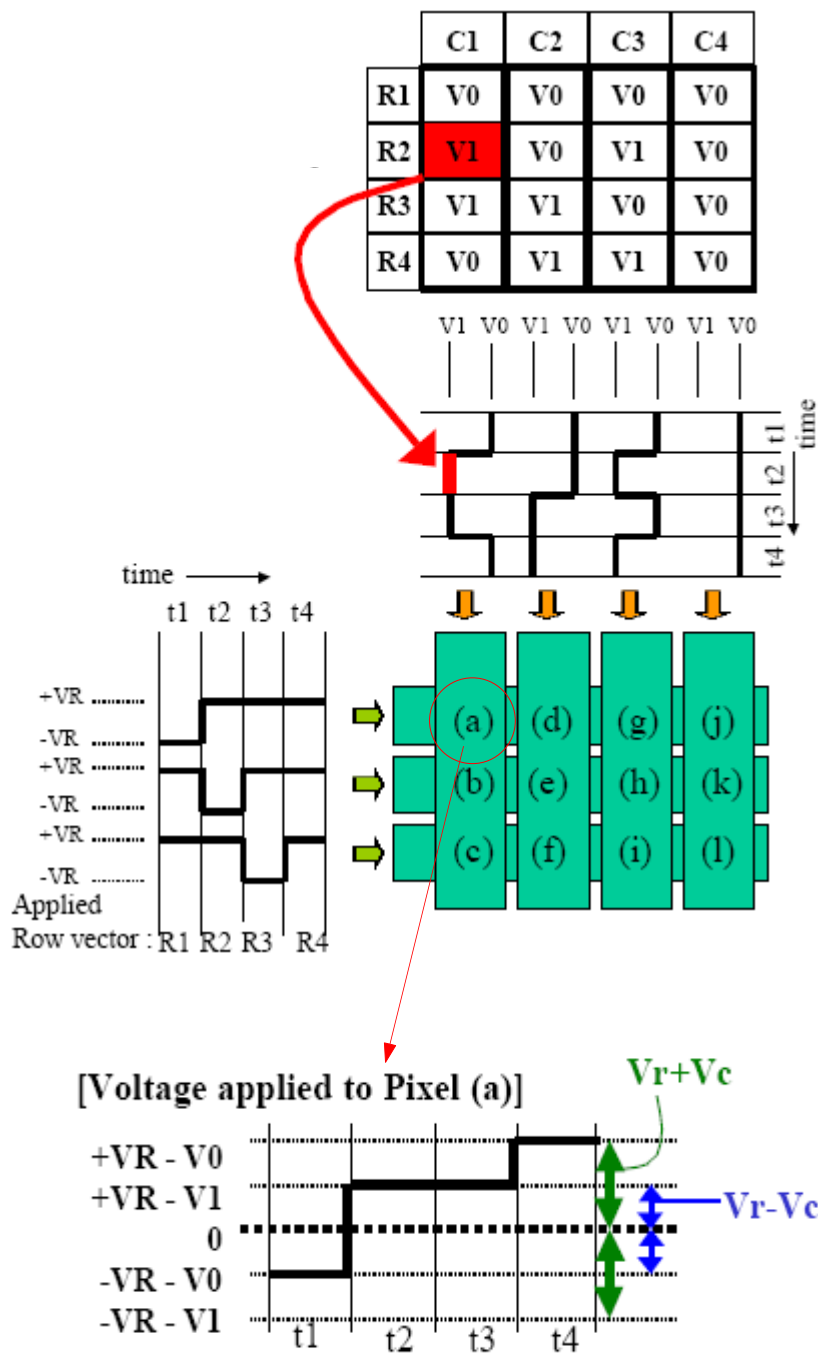


18.4 MLA Calculation (3lines simultaneously selected)

- 1) Count the number of mismatch between the displayed data and row function.
- 2) If the number is 2 or 3, column output is set to V1.
- 3) If the number is 0 or 1, column output is set to V0.

* Example (Case of non-distributed type)





Unit : times

Dot	$Vr + Vc$	$Vr - Vc$	Display	Dot	$Vr + Vc$	$Vr - Vc$	Display
(a)	1	3	off	(g)	1	3	off
(b)	3	1	on	(h)	3	1	on
(c)	3	1	on	(i)	3	1	on
(d)	1	3	off	(j)	1	3	off
(e)	1	3	off	(k)	1	3	off
(f)	3	1	on	(l)	3	1	on