HDC1600

128 X RGB X 160C
COLOR STN Controller - Driver

65K color STN driver embedded Controller & Memory

December 22, 2005

Ver. 0.6

CONTENTS

65K COLOR / 128xRGBx160 OUTPUT LCD DRIVER IC with built-in RAM

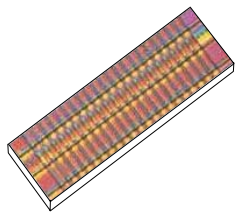
1. INTRODUCTION

HDC1600 is a dot-matrix LCD driver IC with 160 COMMONS and 384 SEGMENTS (128 x RGB) drive ports for 65,536 colors driving. This IC stores the serial or parallel BIT data transferred by the MPU on the built-in RAM (327,680 bits for graphic) and generates the signals to drive LCD panel with on-chip RC oscillator circuits. Also, it is capable of using 8-bit/16-bit data bus alternatively and operating with 68/80-series MPU in asynchronous.

Color graphic display is achieved by selecting 32 gradation levels for R and B, and 64 gradation for G (32R x 64G x 32B = 65,536 color) out of 128 gradation palettes independently.

This IC is suitable for battery-operated system, hand-carrying information equipment by ensuring low power consumption, low power supply and a wide range of operating voltage.

3. EXTERNAL SHAPE



HDC1600

2. FEATURES

LCD Driver Outputs	128 x RGB segments, 160 commons for graphic
Gray Scale Function	65,536 color bitmap LCD driver
Display RAM Capacity	327,680 bits (for graphic usage) Burst RAM write function
Display Mode	Normal display mode : Entire duty displaying, Entire area scrolling Partial display mode : Partial display mode 1, 2 Standby mode
Gradation Scale Display	64 gradation can be selected from 128 gradations by PWM for Green color data 32 gradation can be selected from 128 gradations by PWM for Red and Blue color data
Microprocessor Interface	8-bit/16-bit parallel directly connectable with 68 / 80-series MPU 3/4 Pin interface is selectable (only write operation)
On-chip Low Power Analog Circuit	On-chip RC oscillator, External clock available Built-in voltage booster (programmable) : 6x boosting max. Internal precise reference voltage generator Programmable duty / bias ratio with instruction On-chip Electronic contrast control (256 steps) Temperature compensation (0, -0.05, -0.1, -0.15, -0.2%/ºC selectable)
Operating Voltage Range	Power supply for Logic : 1.8V ~ 3.3V Power supply for Analog and Booster : 2.4V ~ 3.3V LCD driver supply (from booster or external) : 5.0V ~ 16.0V

Various instruction set

display data read/write, display On/Off, positive/negative display, column and row address set, display start line address set, partial display, bias select, boosting coefficient set, all display On/Off, electric volume selection, N-line inversion mode, read modified write, power save…..

Package	COG
Special Features	Non-Volatile Memory for Electronic contrast Calibration : User Trim Built in MPE (Moving Picture Enhancement) algorithm

4. BLOCK DIAGRAM

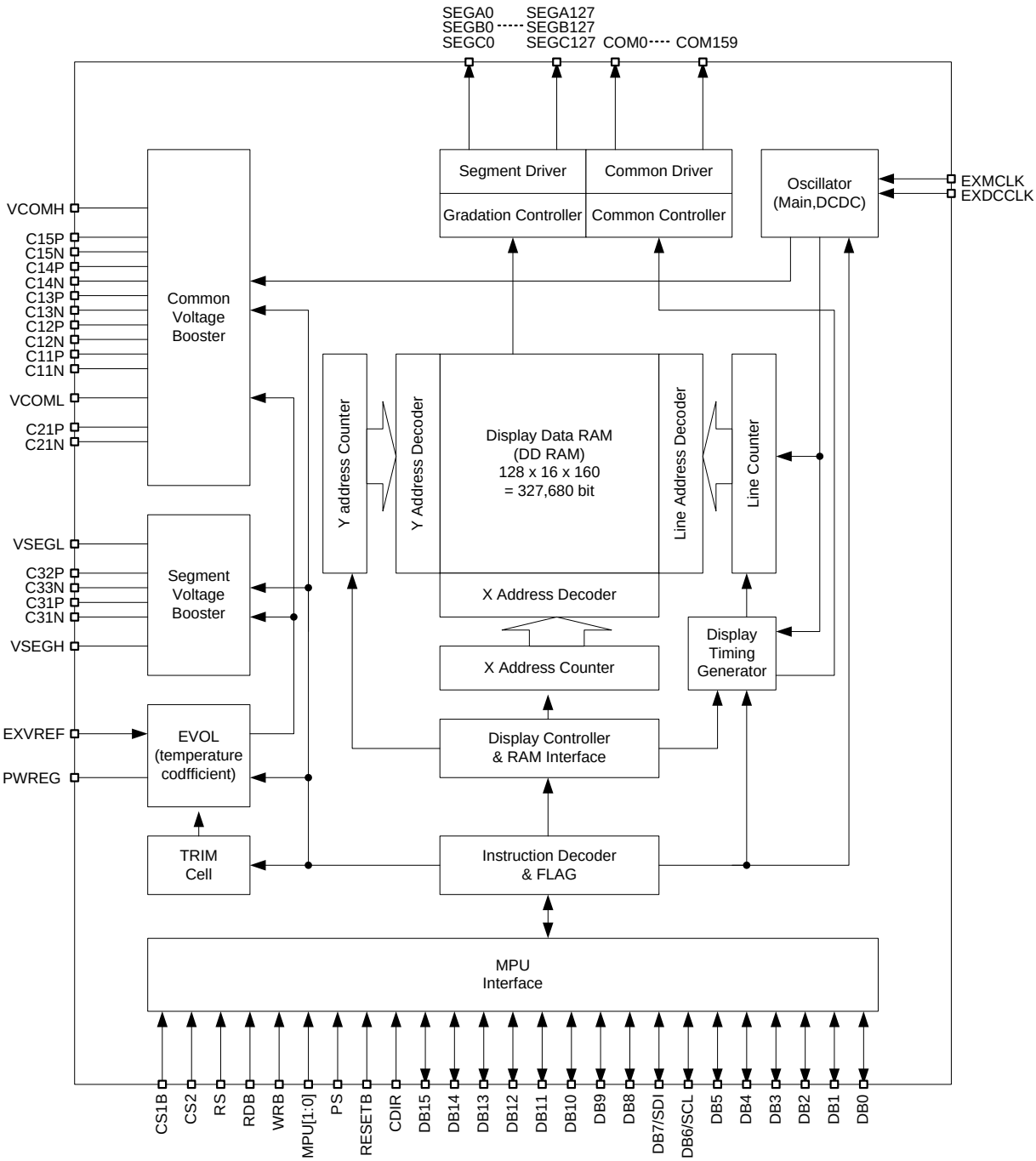
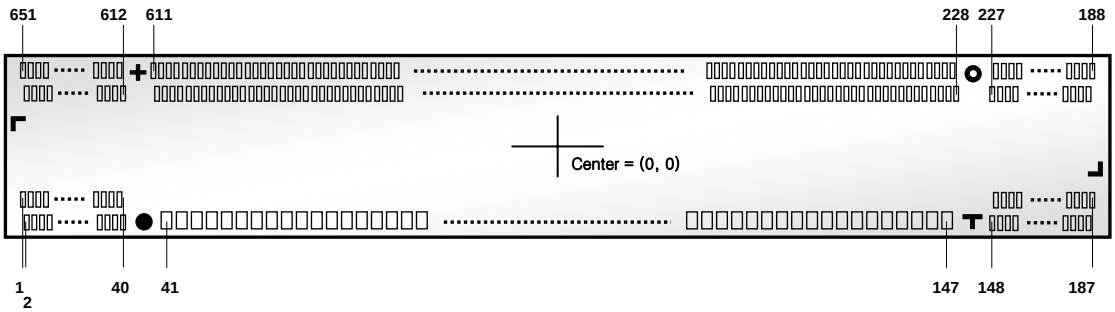


Figure 1. Block Diagram

5. PAD DIMENSIONS

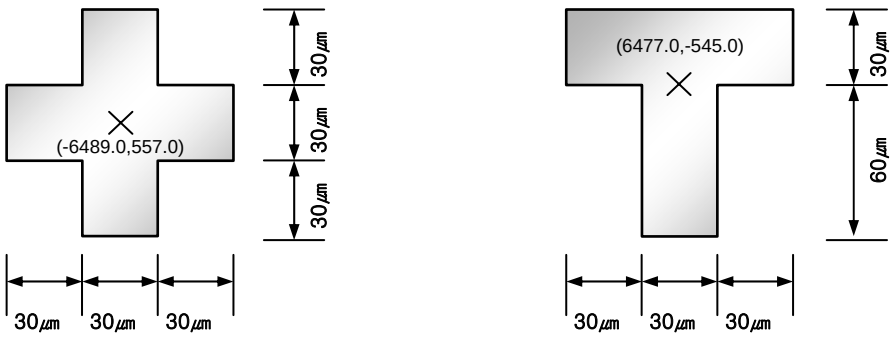
5.1 PAD Location Outline



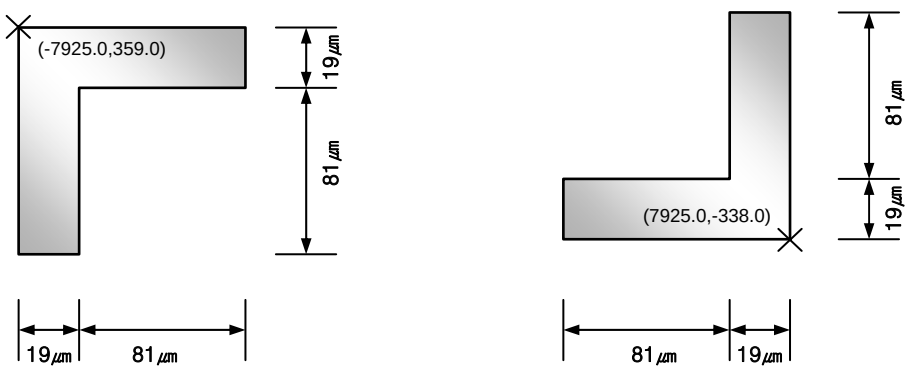
5.2 PAD Dimensions

ITEM	PAD No.	Size		Unit
		X	Y	
Chip Size (without S/L)		15900	1270	㎛
PAD Pitch	1 to 40, 148 to 227 228 to 611, 612 to 651	33.5		
	41 to 147	120		
Bumped PAD Size	1 to 40, 148 to 651	26	97	
	41 to 147	80	60	
Bumped PAD Height	**All pad**	17 ± 1		

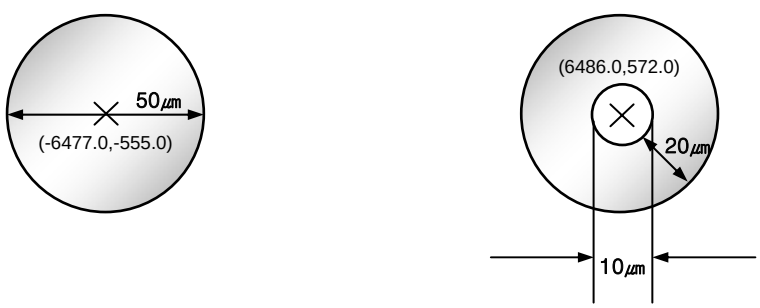
5.3 COG Align Key Coordinates



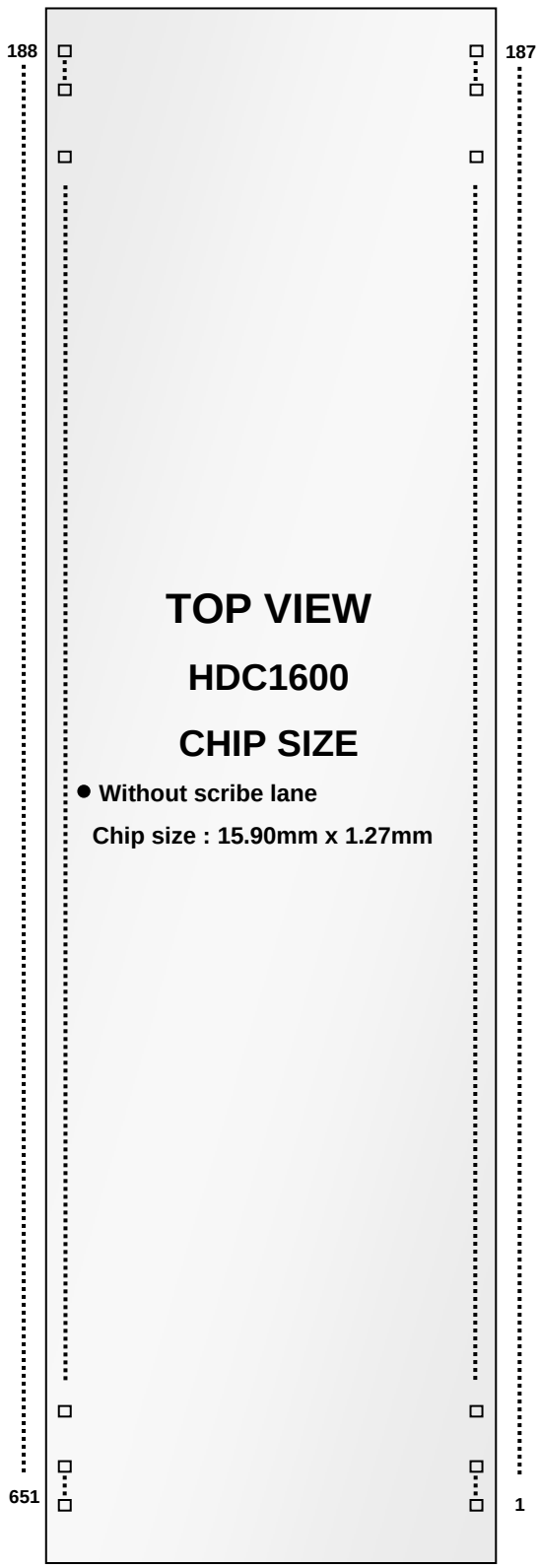
5.4 ILB Align Key Coordinates



5.5 COF Align Key Coordinates



6. PAD LAYOUT



1:COM119
2:COM118
3:COM117
:
38:COM82
39:COM81
40:COM80
41:PS
42:MPU1
43:MPU0
44:CDIR
45:VSS1
46:VDD1
47:CS1B
48:CS2
49:RESETB
50:RS
51:WRB
52:RDB
53:DB0
54:DB1
55:DB2
56:DB3
57:DB4
58:DB5
59:DB6
60:DB7
61:DB8
62:DB9
63:DB10
64:DB11
65:DB12
66:DB13
67:DB14
68:DB15
69:EXMCLK
70:EXMCLK
71:EXDCCLK
72:EXDCCLK
73:CLKO
74:TRIMEN
75:TRCON
76:TST0
77:VREF0
78:EXVREF
79:EXVREF
80:VDD1
81:VDD1
82:VDD1
83:VSS1
84:VSS1
85:VSS1
86:VDD2
87:VDD2
88:VDD2
89:VSS2
90:VSS2
91:VSS2
92:PWREG
93:PWREG
94:VDD3
95:VDD3
96:VDD3
97:VDD3
98:VSS3
99:VSS3
100:VSS3
101:VSS3
102:VCOMH
103:VCOMH
104:VCOMH
105:VCOML
106:VCOML
107:VCOML
108:C11P
109:C11P
110:C11N
111:C11N
112:C12P
113:C12P
114:C12N
115:C12N
116:C13P
117:C13P
118:C13N
119:C13N
120:C14P
121:C14P
122:C14N
123:C14N
124:C15P
125:C15P
126:C15N
127:C15N
128:VSEGH
129:VSEGH
130:VSEGH
131:VSEGL
132:VSEGL
133:VSEGL
134:C21P
135:C21P
136:C21P
137:C21N
138:C21N
139:C21N
140:C31P
141:C31P
142:C31N
143:C31N
144:C32P
145:C32P
146:C32N
147:C32N
148:COM0
149:COM1
150:COM2
:
185:COM37
186:COM38
187:COM39
188:COM40
189:COM41
190:COM42
:
225:COM77
226:COM78
227:COM79
228:SEGC0
229:SEGB0
230:SEGA0
231:SEGC1
232:SEGB1
233:SEGA1
:
609:SEGC127
610:SEGB127
611:SEGA127
612:COM159
613:COM158
614:COM157
:
649:COM122
650:COM121
651:COM120

Figure 2. HDC1600 Chip Pin Configuration

7. PAD COORDINATES

unit : ㎛

NO	PAD NAME	X	Y	NO	PAD NAME	X	Y	NO	PAD NAME	X	Y
1	COM<119>	-7862.25	-409	41	PS	-6362.25	-555	81	VDD1	-1562.25	-555
2	COM<118>	-7828.75	-540	42	MPU1	-6242.25	-555	82	VDD1	-1442.25	-555
3	COM<117>	-7795.25	-409	43	MPU0	-6122.25	-555	83	VSS1	-1322.25	-555
4	COM<116>	-7761.75	-540	44	CDIR	-6002.25	-555	84	VSS1	-1202.25	-555
5	COM<115>	-7728.25	-409	45	VSS1	-5882.25	-555	85	VSS1	-1082.25	-555
6	COM<114>	-7694.75	-540	46	VDD1	-5762.25	-555	86	VDD2	-962.25	-555
7	COM<113>	-7661.25	-409	47	CS1B	-5642.25	-555	87	VDD2	-842.25	-555
8	COM<112>	-7627.75	-540	48	CS2	-5522.25	-555	88	VDD2	-722.25	-555
9	COM<111>	-7594.25	-409	49	RESETB	-5402.25	-555	89	VSS2	-602.25	-555
10	COM<110>	-7560.75	-540	50	RS	-5282.25	-555	90	VSS2	-482.25	-555
11	COM<109>	-7527.25	-409	51	WRB	-5162.25	-555	91	VSS2	-362.25	-555
12	COM<108>	-7493.75	-540	52	RDB	-5042.25	-555	92	PWREG	-242.25	-555
13	COM<107>	-7460.25	-409	53	DB<0>	-4922.25	-555	93	PWREG	-122.25	-555
14	COM<106>	-7426.75	-540	54	DB<1>	-4802.25	-555	94	VDD3	-2.25	-555
15	COM<105>	-7393.25	-409	55	DB<2>	-4682.25	-555	95	VDD3	117.75	-555
16	COM<104>	-7359.75	-540	56	DB<3>	-4562.25	-555	96	VDD3	237.75	-555
17	COM<103>	-7326.25	-409	57	DB<4>	-4442.25	-555	97	VDD3	357.75	-555
18	COM<102>	-7292.75	-540	58	DB<5>	-4322.25	-555	98	VSS3	477.75	-555
19	COM<101>	-7259.25	-409	59	DB<6>	-4202.25	-555	99	VSS3	597.75	-555
20	COM<100>	-7225.75	-540	60	DB<7>	-4082.25	-555	100	VSS3	717.75	-555
21	COM<99>	-7192.25	-409	61	DB<8>	-3962.25	-555	101	VSS3	837.75	-555
22	COM<98>	-7158.75	-540	62	DB<9>	-3842.25	-555	102	VCOMH	957.75	-555
23	COM<97>	-7125.25	-409	63	DB<10>	-3722.25	-555	103	VCOMH	1077.75	-555
24	COM<96>	-7091.75	-540	64	DB<11>	-3602.25	-555	104	VCOMH	1197.75	-555
25	COM<95>	-7058.25	-409	65	DB<12>	-3482.25	-555	105	VCOML	1317.75	-555
26	COM<94>	-7024.75	-540	66	DB<13>	-3362.25	-555	106	VCOML	1437.75	-555
27	COM<93>	-6991.25	-409	67	DB<14>	-3242.25	-555	107	VCOML	1557.75	-555
28	COM<92>	-6957.75	-540	68	DB<15>	-3122.25	-555	108	C11P	1677.75	-555
29	COM<91>	-6924.25	-409	69	EXMCLK	-3002.25	-555	109	C11P	1797.75	-555
30	COM<90>	-6890.75	-540	70	EXMCLK	-2882.25	-555	110	C11N	1917.75	-555
31	COM<89>	-6857.25	-409	71	EXDCCLK	-2762.25	-555	111	C11N	2037.75	-555
32	COM<88>	-6823.75	-540	72	EXDCCLK	-2642.25	-555	112	C12P	2157.75	-555
33	COM<87>	-6790.25	-409	73	CLKO	-2522.25	-555	113	C12P	2277.75	-555
34	COM<86>	-6756.75	-540	74	TRIMEN	-2402.25	-555	114	C12N	2397.75	-555
35	COM<85>	-6723.25	-409	75	TRCON	-2282.25	-555	115	C12N	2517.75	-555
36	COM<84>	-6689.75	-540	76	TSTO0	-2162.25	-555	116	C13P	2637.75	-555
37	COM<83>	-6656.25	-409	77	VREF0	-2042.25	-555	117	C13P	2757.75	-555
38	COM<82>	-6622.75	-540	78	EXVREF	-1922.25	-555	118	C13N	2877.75	-555
39	COM<81>	-6589.25	-409	79	EXVREF	-1802.25	-555	119	C13N	2997.75	-555
40	COM<80>	-6555.75	-540	80	VDD1	-1682.25	-555	120	C14P	3117.75	-555

(Continued) unit : ㎛

NO	PAD NAME	X	Y	NO	PAD NAME	X	Y	NO	PAD NAME	X	Y
121	C14P	3237.75	-555	161	COM<13>	6991.25	-409	201	COM<53>	7426.75	424.5
122	C14N	3357.75	-555	162	COM<14>	7024.75	-540	202	COM<54>	7393.25	555.5
123	C14N	3477.75	-555	163	COM<15>	7058.25	-409	203	COM<55>	7359.75	424.5
124	C15P	3597.75	-555	164	COM<16>	7091.75	-540	204	COM<56>	7326.25	555.5
125	C15P	3717.75	-555	165	COM<17>	7125.25	-409	205	COM<57>	7292.75	424.5
126	C15N	3837.75	-555	166	COM<18>	7158.75	-540	206	COM<58>	7259.25	555.5
127	C15N	3957.75	-555	167	COM<19>	7192.25	-409	207	COM<59>	7225.75	424.5
128	VSEGH	4077.75	-555	168	COM<20>	7225.75	-540	208	COM<60>	7192.25	555.5
129	VSEGH	4197.75	-555	169	COM<21>	7259.25	-409	209	COM<61>	7158.75	424.5
130	VSEGH	4317.75	-555	170	COM<22>	7292.75	-540	210	COM<62>	7125.25	555.5
131	VSEGL	4437.75	-555	171	COM<23>	7326.25	-409	211	COM<63>	7091.75	424.5
132	VSEGL	4557.75	-555	172	COM<24>	7359.75	-540	212	COM<64>	7058.25	555.5
133	VSEGL	4677.75	-555	173	COM<25>	7393.25	-409	213	COM<65>	7024.75	424.5
134	C21P	4797.75	-555	174	COM<26>	7426.75	-540	214	COM<66>	6991.25	555.5
135	C21P	4917.75	-555	175	COM<27>	7460.25	-409	215	COM<67>	6957.75	424.5
136	C21P	5037.75	-555	176	COM<28>	7493.75	-540	216	COM<68>	6924.25	555.5
137	C21N	5157.75	-555	177	COM<29>	7527.25	-409	217	COM<69>	6890.75	424.5
138	C21N	5277.75	-555	178	COM<30>	7560.75	-540	218	COM<70>	6857.25	555.5
139	C21N	5397.75	-555	179	COM<31>	7594.25	-409	219	COM<71>	6823.75	424.5
140	C31P	5517.75	-555	180	COM<32>	7627.75	-540	220	COM<72>	6790.25	555.5
141	C31P	5637.75	-555	181	COM<33>	7661.25	-409	221	COM<73>	6756.75	424.5
142	C31N	5757.75	-555	182	COM<34>	7694.75	-540	222	COM<74>	6723.25	555.5
143	C31N	5877.75	-555	183	COM<35>	7728.25	-409	223	COM<75>	6689.75	424.5
144	C32P	5997.75	-555	184	COM<36>	7761.75	-540	224	COM<76>	6656.25	555.5
145	C32P	6117.75	-555	185	COM<37>	7795.25	-409	225	COM<77>	6622.75	424.5
146	C32N	6237.75	-555	186	COM<38>	7828.75	-540	226	COM<78>	6589.25	555.5
147	C32N	6357.75	-555	187	COM<39>	7862.25	-409	227	COM<79>	6555.75	424.5
148	COM<0>	6555.75	-540	188	COM<40>	7862.25	555.5	228	SEGC<0>	6415.25	424.5
149	COM<1>	6589.25	-409	189	COM<41>	7828.75	424.5	229	SEGB<0>	6381.75	555.5
150	COM<2>	6622.75	-540	190	COM<42>	7795.25	555.5	230	SEGA<0>	6348.25	424.5
151	COM<3>	6656.25	-409	191	COM<43>	7761.75	424.5	231	SEGC<1>	6314.75	555.5
152	COM<4>	6689.75	-540	192	COM<44>	7728.25	555.5	232	SEGB<1>	6281.25	424.5
153	COM<5>	6723.25	-409	193	COM<45>	7694.75	424.5	233	SEGA<1>	6247.75	555.5
154	COM<6>	6756.75	-540	194	COM<46>	7661.25	555.5	234	SEGC<2>	6214.25	424.5
155	COM<7>	6790.25	-409	195	COM<47>	7627.75	424.5	235	SEGB<2>	6180.75	555.5
156	COM<8>	6823.75	-540	196	COM<48>	7594.25	555.5	236	SEGA<2>	6147.25	424.5
157	COM<9>	6857.25	-409	197	COM<49>	7560.75	424.5	237	SEGC<3>	6113.75	555.5
158	COM<10>	6890.75	-540	198	COM<50>	7527.25	555.5	238	SEGB<3>	6080.25	424.5
159	COM<11>	6924.25	-409	199	COM<51>	7493.75	424.5	239	SEGA<3>	6046.75	555.5
160	COM<12>	6957.75	-540	200	COM<52>	7460.25	555.5	240	SEGC<4>	6013.25	424.5

(Continued) unit : ㎛

NO	PAD NAME	X	Y	NO	PAD NAME	X	Y	NO	PAD NAME	X	Y
241	SEGB<4>	5979.75	555.5	281	SEGA<17>	4639.75	555.5	321	SEGC<31>	3299.75	555.5
242	SEGA<4>	5946.25	424.5	282	SEGC<18>	4606.25	424.5	322	SEGB<31>	3266.25	424.5
243	SEGC<5>	5912.75	555.5	283	SEGB<18>	4572.75	555.5	323	SEGA<31>	3232.75	555.5
244	SEGB<5>	5879.25	424.5	284	SEGA<18>	4539.25	424.5	324	SEGC<32>	3199.25	424.5
245	SEGA<5>	5845.75	555.5	285	SEGC<19>	4505.75	555.5	325	SEGB<32>	3165.75	555.5
246	SEGC<6>	5812.25	424.5	286	SEGB<19>	4472.25	424.5	326	SEGA<32>	3132.25	424.5
247	SEGB<6>	5778.75	555.5	287	SEGA<19>	4438.75	555.5	327	SEGC<33>	3098.75	555.5
248	SEGA<6>	5745.25	424.5	288	SEGC<20>	4405.25	424.5	328	SEGB<33>	3065.25	424.5
249	SEGC<7>	5711.75	555.5	289	SEGB<20>	4371.75	555.5	329	SEGA<33>	3031.75	555.5
250	SEGB<7>	5678.25	424.5	290	SEGA<20>	4338.25	424.5	330	SEGC<34>	2998.25	424.5
251	SEGA<7>	5644.75	555.5	291	SEGC<21>	4304.75	555.5	331	SEGB<34>	2964.75	555.5
252	SEGC<8>	5611.25	424.5	292	SEGB<21>	4271.25	424.5	332	SEGA<34>	2931.25	424.5
253	SEGB<8>	5577.75	555.5	293	SEGA<21>	4237.75	555.5	333	SEGC<35>	2897.75	555.5
254	SEGA<8>	5544.25	424.5	294	SEGC<22>	4204.25	424.5	334	SEGB<35>	2864.25	424.5
255	SEGC<9>	5510.75	555.5	295	SEGB<22>	4170.75	555.5	335	SEGA<35>	2830.75	555.5
256	SEGB<9>	5477.25	424.5	296	SEGA<22>	4137.25	424.5	336	SEGC<36>	2797.25	424.5
257	SEGA<9>	5443.75	555.5	297	SEGC<23>	4103.75	555.5	337	SEGB<36>	2763.75	555.5
258	SEGC<10>	5410.25	424.5	298	SEGB<23>	4070.25	424.5	338	SEGA<36>	2730.25	424.5
259	SEGB<10>	5376.75	555.5	299	SEGA<23>	4036.75	555.5	339	SEGC<37>	2696.75	555.5
260	SEGA<10>	5343.25	424.5	300	SEGC<24>	4003.25	424.5	340	SEGB<37>	2663.25	424.5
261	SEGC<11>	5309.75	555.5	301	SEGB<24>	3969.75	555.5	341	SEGA<37>	2629.75	555.5
262	SEGB<11>	5276.25	424.5	302	SEGA<24>	3936.25	424.5	342	SEGC<38>	2596.25	424.5
263	SEGA<11>	5242.75	555.5	303	SEGC<25>	3902.75	555.5	343	SEGB<38>	2562.75	555.5
264	SEGC<12>	5209.25	424.5	304	SEGB<25>	3869.25	424.5	344	SEGA<38>	2529.25	424.5
265	SEGB<12>	5175.75	555.5	305	SEGA<25>	3835.75	555.5	345	SEGC<39>	2495.75	555.5
266	SEGA<12>	5142.25	424.5	306	SEGC<26>	3802.25	424.5	346	SEGB<39>	2462.25	424.5
267	SEGC<13>	5108.75	555.5	307	SEGB<26>	3768.75	555.5	347	SEGA<39>	2428.75	555.5
268	SEGB<13>	5075.25	424.5	308	SEGA<26>	3735.25	424.5	348	SEGC<40>	2395.25	424.5
269	SEGA<13>	5041.75	555.5	309	SEGC<27>	3701.75	555.5	349	SEGB<40>	2361.75	555.5
270	SEGC<14>	5008.25	424.5	310	SEGB<27>	3668.25	424.5	350	SEGA<40>	2328.25	424.5
271	SEGB<14>	4974.75	555.5	311	SEGA<27>	3634.75	555.5	351	SEGC<41>	2294.75	555.5
272	SEGA<14>	4941.25	424.5	312	SEGC<28>	3601.25	424.5	352	SEGB<41>	2261.25	424.5
273	SEGC<15>	4907.75	555.5	313	SEGB<28>	3567.75	555.5	353	SEGA<41>	2227.75	555.5
274	SEGB<15>	4874.25	424.5	314	SEGA<28>	3534.25	424.5	354	SEGC<42>	2194.25	424.5
275	SEGA<15>	4840.75	555.5	315	SEGC<29>	3500.75	555.5	355	SEGB<42>	2160.75	555.5
276	SEGC<16>	4807.25	424.5	316	SEGB<29>	3467.25	424.5	356	SEGA<42>	2127.25	424.5
277	SEGB<16>	4773.75	555.5	317	SEGA<29>	3433.75	555.5	357	SEGC<43>	2093.75	555.5
278	SEGA<16>	4740.25	424.5	318	SEGC<30>	3400.25	424.5	358	SEGB<43>	2060.25	424.5
279	SEGC<17>	4706.75	555.5	319	SEGB<30>	3366.75	555.5	359	SEGA<43>	2026.75	555.5
280	SEGB<17>	4673.25	424.5	320	SEGA<30>	3333.25	424.5	360	SEGC<44>	1993.25	424.5

(Continued) unit : ㎛

NO	PAD NAME	X	Y	NO	PAD NAME	X	Y	NO	PAD NAME	X	Y
361	SEGB<44>	1959.75	555.5	401	SEGA<57>	619.75	555.5	441	SEGC<71>	-720.25	555.5
362	SEGA<44>	1926.25	424.5	402	SEGC<58>	586.25	424.5	442	SEGB<71>	-753.75	424.5
363	SEGC<45>	1892.75	555.5	403	SEGB<58>	552.75	555.5	443	SEGA<71>	-787.25	555.5
364	SEGB<45>	1859.25	424.5	404	SEGA<58>	519.25	424.5	444	SEGC<72>	-820.75	424.5
365	SEGA<45>	1825.75	555.5	405	SEGC<59>	485.75	555.5	445	SEGB<72>	-854.25	555.5
366	SEGC<46>	1792.25	424.5	406	SEGB<59>	452.25	424.5	446	SEGA<72>	-887.75	424.5
367	SEGB<46>	1758.75	555.5	407	SEGA<59>	418.75	555.5	447	SEGC<73>	-921.25	555.5
368	SEGA<46>	1725.25	424.5	408	SEGC<60>	385.25	424.5	448	SEGB<73>	-954.75	424.5
369	SEGC<47>	1691.75	555.5	409	SEGB<60>	351.75	555.5	449	SEGA<73>	-988.25	555.5
370	SEGB<47>	1658.25	424.5	410	SEGA<60>	318.25	424.5	450	SEGC<74>	-1021.75	424.5
371	SEGA<47>	1624.75	555.5	411	SEGC<61>	284.75	555.5	451	SEGB<74>	-1055.25	555.5
372	SEGC<48>	1591.25	424.5	412	SEGB<61>	251.25	424.5	452	SEGA<74>	-1088.75	424.5
373	SEGB<48>	1557.75	555.5	413	SEGA<61>	217.75	555.5	453	SEGC<75>	-1122.25	555.5
374	SEGA<48>	1524.25	424.5	414	SEGC<62>	184.25	424.5	454	SEGB<75>	-1155.75	424.5
375	SEGC<49>	1490.75	555.5	415	SEGB<62>	150.75	555.5	455	SEGA<75>	-1189.25	555.5
376	SEGB<49>	1457.25	424.5	416	SEGA<62>	117.25	424.5	456	SEGC<76>	-1222.75	424.5
377	SEGA<49>	1423.75	555.5	417	SEGC<63>	83.75	555.5	457	SEGB<76>	-1256.25	555.5
378	SEGC<50>	1390.25	424.5	418	SEGB<63>	50.25	424.5	458	SEGA<76>	-1289.75	424.5
379	SEGB<50>	1356.75	555.5	419	SEGA<63>	16.75	555.5	459	SEGC<77>	-1323.25	555.5
380	SEGA<50>	1323.25	424.5	420	SEGC<64>	-16.75	424.5	460	SEGB<77>	-1356.75	424.5
381	SEGC<51>	1289.75	555.5	421	SEGB<64>	-50.25	555.5	461	SEGA<77>	-1390.25	555.5
382	SEGB<51>	1256.25	424.5	422	SEGA<64>	-83.75	424.5	462	SEGC<78>	-1423.75	424.5
383	SEGA<51>	1222.75	555.5	423	SEGC<65>	-117.25	555.5	463	SEGB<78>	-1457.25	555.5
384	SEGC<52>	1189.25	424.5	424	SEGB<65>	-150.75	424.5	464	SEGA<78>	-1490.75	424.5
385	SEGB<52>	1155.75	555.5	425	SEGA<65>	-184.25	555.5	465	SEGC<79>	-1524.25	555.5
386	SEGA<52>	1122.25	424.5	426	SEGC<66>	-217.75	424.5	466	SEGB<79>	-1557.75	424.5
387	SEGC<53>	1088.75	555.5	427	SEGB<66>	-251.25	555.5	467	SEGA<79>	-1591.25	555.5
388	SEGB<53>	1055.25	424.5	428	SEGA<66>	-284.75	424.5	468	SEGC<80>	-1624.75	424.5
389	SEGA<53>	1021.75	555.5	429	SEGC<67>	-318.25	555.5	469	SEGB<80>	-1658.25	555.5
390	SEGC<54>	988.25	424.5	430	SEGB<67>	-351.75	424.5	470	SEGA<80>	-1691.75	424.5
391	SEGB<54>	954.75	555.5	431	SEGA<67>	-385.25	555.5	471	SEGC<81>	-1725.25	555.5
392	SEGA<54>	921.25	424.5	432	SEGC<68>	-418.75	424.5	472	SEGB<81>	-1758.75	424.5
393	SEGC<55>	887.75	555.5	433	SEGB<68>	-452.25	555.5	473	SEGA<81>	-1792.25	555.5
394	SEGB<55>	854.25	424.5	434	SEGA<68>	-485.75	424.5	474	SEGC<82>	-1825.75	424.5
395	SEGA<55>	820.75	555.5	435	SEGC<69>	-519.25	555.5	475	SEGB<82>	-1859.25	555.5
396	SEGC<56>	787.25	424.5	436	SEGB<69>	-552.75	424.5	476	SEGA<82>	-1892.75	424.5
397	SEGB<56>	753.75	555.5	437	SEGA<69>	-586.25	555.5	477	SEGC<83>	-1926.25	555.5
398	SEGA<56>	720.25	424.5	438	SEGC<70>	-619.75	424.5	478	SEGB<83>	-1959.75	424.5
399	SEGC<57>	686.75	555.5	439	SEGB<70>	-653.25	555.5	479	SEGA<83>	-1993.25	555.5
400	SEGB<57>	653.25	424.5	440	SEGA<70>	-686.75	424.5	480	SEGC<84>	-2026.75	424.5

(Continued) unit : ㎛

NO	PAD NAME	X	Y	NO	PAD NAME	X	Y	NO	PAD NAME	X	Y
481	SEGB<84>	-2060.25	555.5	521	SEGA<97>	-3400.25	555.5	561	SEGC<111>	-4740.25	555.5
482	SEGA<84>	-2093.75	424.5	522	SEGC<98>	-3433.75	424.5	562	SEGB<111>	-4773.75	424.5
483	SEGC<85>	-2127.25	555.5	523	SEGB<98>	-3467.25	555.5	563	SEGA<111>	-4807.25	555.5
484	SEGB<85>	-2160.75	424.5	524	SEGA<98>	-3500.75	424.5	564	SEGC<112>	-4840.75	424.5
485	SEGA<85>	-2194.25	555.5	525	SEGC<99>	-3534.25	555.5	565	SEGB<112>	-4874.25	555.5
486	SEGC<86>	-2227.75	424.5	526	SEGB<99>	-3567.75	424.5	566	SEGA<112>	-4907.75	424.5
487	SEGB<86>	-2261.25	555.5	527	SEGA<99>	-3601.25	555.5	567	SEGC<113>	-4941.25	555.5
488	SEGA<86>	-2294.75	424.5	528	SEGC<100>	-3634.75	424.5	568	SEGB<113>	-4974.75	424.5
489	SEGC<87>	-2328.25	555.5	529	SEGB<100>	-3668.25	555.5	569	SEGA<113>	-5008.25	555.5
490	SEGB<87>	-2361.75	424.5	530	SEGA<100>	-3701.75	424.5	570	SEGC<114>	-5041.75	424.5
491	SEGA<87>	-2395.25	555.5	531	SEGC<101>	-3735.25	555.5	571	SEGB<114>	-5075.25	555.5
492	SEGC<88>	-2428.75	424.5	532	SEGB<101>	-3768.75	424.5	572	SEGA<114>	-5108.75	424.5
493	SEGB<88>	-2462.25	555.5	533	SEGA<101>	-3802.25	555.5	573	SEGC<115>	-5142.25	555.5
494	SEGA<88>	-2495.75	424.5	534	SEGC<102>	-3835.75	424.5	574	SEGB<115>	-5175.75	424.5
495	SEGC<89>	-2529.25	555.5	535	SEGB<102>	-3869.25	555.5	575	SEGA<115>	-5209.25	555.5
496	SEGB<89>	-2562.75	424.5	536	SEGA<102>	-3902.75	424.5	576	SEGC<116>	-5242.75	424.5
497	SEGA<89>	-2596.25	555.5	537	SEGC<103>	-3936.25	555.5	577	SEGB<116>	-5276.25	555.5
498	SEGC<90>	-2629.75	424.5	538	SEGB<103>	-3969.75	424.5	578	SEGA<116>	-5309.75	424.5
499	SEGB<90>	-2663.25	555.5	539	SEGA<103>	-4003.25	555.5	579	SEGC<117>	-5343.25	555.5
500	SEGA<90>	-2696.75	424.5	540	SEGC<104>	-4036.75	424.5	580	SEGB<117>	-5376.75	424.5
501	SEGC<91>	-2730.25	555.5	541	SEGB<104>	-4070.25	555.5	581	SEGA<117>	-5410.25	555.5
502	SEGB<91>	-2763.75	424.5	542	SEGA<104>	-4103.75	424.5	582	SEGC<118>	-5443.75	424.5
503	SEGA<91>	-2797.25	555.5	543	SEGC<105>	-4137.25	555.5	583	SEGB<118>	-5477.25	555.5
504	SEGC<92>	-2830.75	424.5	544	SEGB<105>	-4170.75	424.5	584	SEGA<118>	-5510.75	424.5
505	SEGB<92>	-2864.25	555.5	545	SEGA<105>	-4204.25	555.5	585	SEGC<119>	-5544.25	555.5
506	SEGA<92>	-2897.75	424.5	546	SEGC<106>	-4237.75	424.5	586	SEGB<119>	-5577.75	424.5
507	SEGC<93>	-2931.25	555.5	547	SEGB<106>	-4271.25	555.5	587	SEGA<119>	-5611.25	555.5
508	SEGB<93>	-2964.75	424.5	548	SEGA<106>	-4304.75	424.5	588	SEGC<120>	-5644.75	424.5
509	SEGA<93>	-2998.25	555.5	549	SEGC<107>	-4338.25	555.5	589	SEGB<120>	-5678.25	555.5
510	SEGC<94>	-3031.75	424.5	550	SEGB<107>	-4371.75	424.5	590	SEGA<120>	-5711.75	424.5
511	SEGB<94>	-3065.25	555.5	551	SEGA<107>	-4405.25	555.5	591	SEGC<121>	-5745.25	555.5
512	SEGA<94>	-3098.75	424.5	552	SEGC<108>	-4438.75	424.5	592	SEGB<121>	-5778.75	424.5
513	SEGC<95>	-3132.25	555.5	553	SEGB<108>	-4472.25	555.5	593	SEGA<121>	-5812.25	555.5
514	SEGB<95>	-3165.75	424.5	554	SEGA<108>	-4505.75	424.5	594	SEGC<122>	-5845.75	424.5
515	SEGA<95>	-3199.25	555.5	555	SEGC<109>	-4539.25	555.5	595	SEGB<122>	-5879.25	555.5
516	SEGC<96>	-3232.75	424.5	556	SEGB<109>	-4572.75	424.5	596	SEGA<122>	-5912.75	424.5
517	SEGB<96>	-3266.25	555.5	557	SEGA<109>	-4606.25	555.5	597	SEGC<123>	-5946.25	555.5
518	SEGA<96>	-3299.75	424.5	558	SEGC<110>	-4639.75	424.5	598	SEGB<123>	-5979.75	424.5
519	SEGC<97>	-3333.25	555.5	559	SEGB<110>	-4673.25	555.5	599	SEGA<123>	-6013.25	555.5
520	SEGB<97>	-3366.75	424.5	560	SEGA<110>	-4706.75	424.5	600	SEGC<124>	-6046.75	424.5

(Continued) unit : ㎛

NO	PAD NAME	X	Y	NO	PAD NAME	X	Y
601	SEGB<124>	-6080.25	555.5	641	COM<130>	-7527.25	555.5
602	SEGA<124>	-6113.75	424.5	642	COM<129>	-7560.75	424.5
603	SEGC<125>	-6147.25	555.5	643	COM<128>	-7594.25	555.5
604	SEGB<125>	-6180.75	424.5	644	COM<127>	-7627.75	424.5
605	SEGA<125>	-6214.25	555.5	645	COM<126>	-7661.25	555.5
606	SEGC<126>	-6247.75	424.5	646	COM<125>	-7694.75	424.5
607	SEGB<126>	-6281.25	555.5	647	COM<124>	-7728.25	555.5
608	SEGA<126>	-6314.75	424.5	648	COM<123>	-7761.75	424.5
609	SEGC<127>	-6348.25	555.5	649	COM<122>	-7795.25	555.5
610	SEGB<127>	-6381.75	424.5	650	COM<121>	-7828.75	424.5
611	SEGA<127>	-6415.25	555.5	651	COM<120>	-7862.25	555.5
612	COM<159>	-6555.75	424.5				
613	COM<158>	-6589.25	555.5				
614	COM<157>	-6622.75	424.5				
615	COM<156>	-6656.25	555.5				
616	COM<155>	-6689.75	424.5				
617	COM<154>	-6723.25	555.5				
618	COM<153>	-6756.75	424.5				
619	COM<152>	-6790.25	555.5				
620	COM<151>	-6823.75	424.5				
621	COM<150>	-6857.25	555.5				
622	COM<149>	-6890.75	424.5				
623	COM<148>	-6924.25	555.5				
624	COM<147>	-6957.75	424.5				
625	COM<146>	-6991.25	555.5				
626	COM<145>	-7024.75	424.5				
627	COM<144>	-7058.25	555.5				
628	COM<143>	-7091.75	424.5				
629	COM<142>	-7125.25	555.5				
630	COM<141>	-7158.75	424.5				
631	COM<140>	-7192.25	555.5				
632	COM<139>	-7225.75	424.5				
633	COM<138>	-7259.25	555.5				
634	COM<137>	-7292.75	424.5				
635	COM<136>	-7326.25	555.5				
636	COM<135>	-7359.75	424.5				
637	COM<134>	-7393.25	555.5				
638	COM<133>	-7426.75	424.5				
639	COM<132>	-7460.25	555.5				
640	COM<131>	-7493.75	424.5				

8. PIN DESCRIPTION

8.1 Power Supply Pins

PIN	NAME	I/O	Description
	VDD1	Supply	Logic power supply.
	VDD2	Supply	Analog power supply.
	VDD3	Supply	Voltage booster power supply.
	VSS1	Supply	Logic ground.
	VSS2	Supply	Analog ground.
	VSS3	Supply	Voltage booster ground.
	VCOMH	Supply I / O	LCD common high selected driving voltage input / output pin.
	VCOML	Supply I / O	LCD common low selected driving voltage input / output pin.
	VSEGH	Supply I / O	LCD segment high selected driving voltage input / output pin.
	VSEGL	Supply I / O	LCD segment low selected driving voltage input / output pin. When external power is used, voltage should have following relations. VCOMH > VSEGH > VSS1 > VSEGL > VCOML (VCOMH – VSS1 = VSS1 – VCOML, VSEGH – VSS1 = VSS1 – VSEGL) VCOMH, VCOML, VSEGH, VSEGL voltages are generated by voltage booster under dcdc circuits is ON. When internal power supply is used, capacitors must be connected between VCOMH, VCOML, VCOMH, VCOML and VSS1.
	C11P / C11N C12P / C12N C13P / C13N C14P / C14N C15P / C15N	Supply I / O	External capacitor connection pins for 1’st voltage booster.
	C21P / C21N	Supply I / O	External capacitor connection pins for 2’nd voltage booster.
	C31P / C31N C32P / C32N	Supply I / O	External capacitor connection pins for 3’rd voltage booster.
	PWREG	Supply I / O	External capacitor connection pins for internal reference voltage power. The regulator output is as a power supplier for an internal reference voltage block.

8.2 MPU Interface Pins

<table>
<tr><th>PIN</th><th>NAME</th><th>I/O</th><th>Description</th></tr>
<tr><td></td><td>RESETB</td><td>I</td><td>Reset input pin.
When RESETB is “L”, initialization is executed.</td></tr>
<tr><td></td><td>CS1B
CS2</td><td>I</td><td>Chip selection input pins.
Data, instruction I/O is enabled only CS1B is “L” and CS2 is “H”.
When chip select is non-active, DB[15:0] may be high impedance.</td></tr>
<tr><td></td><td>RS</td><td>I</td><td>Data / Instruction select input pin.
<table>
<tr><th>RS</th><th>Description</th></tr>
<tr><td>L</td><td>DB7 ~ DB0 are instruction data</td></tr>
<tr><td>H</td><td>DB15 ~ DB0 are display data</td></tr>
</table></td></tr>
<tr><td></td><td>PS
MPU[1:0]</td><td>I</td><td>MPU interface select pins.
<table>
<tr><th>PS</th><th>MPU[1]</th><th>MPU[0]</th><th>Description</th></tr>
<tr><td rowspan="4">H</td><td rowspan="2">L</td><td>L</td><td>8080-series 8bit interface</td></tr>
<tr><td>H</td><td>8080-series 16bit interface</td></tr>
<tr><td rowspan="2">H</td><td>L</td><td>6800-series 8bit interface</td></tr>
<tr><td>H</td><td>6800-series 16bit interface</td></tr>
<tr><td rowspan="4">L</td><td rowspan="2">L</td><td>L</td><td>3 pin 8bit SPI (Write only)</td></tr>
<tr><td>H</td><td>3 pin 16bit SPI (Write only)</td></tr>
<tr><td rowspan="2">H</td><td>L</td><td>4 pin 8bit SPI (Write only)</td></tr>
<tr><td>H</td><td>4 pin 16bit SPI (Write only)</td></tr>
</table></td></tr>
<tr><td></td><td>WRB
(R/W)</td><td>I</td><td>Read / Write execution control pin.
<table>
<tr><th>PS</th><th>MPU[1]</th><th>MPU Type</th><th>WRB</th><th>Description</th></tr>
<tr><td>H</td><td>L</td><td>8080 series</td><td>WRB</td><td>Write enable clock input pin.
The data on DB[15:0] are latched
at the rising edge of the WRB signal.</td></tr>
<tr><td>H</td><td>H</td><td>6800 series</td><td>R/W</td><td>Read / Write control input pin.
-R/W = “H” : read
-R/W = “L” : write</td></tr>
</table></td></tr>
<tr><td></td><td>RDB
(E)</td><td>I</td><td>Read / Write execution control pin.
<table>
<tr><th>PS</th><th>MPU[1]</th><th>MPU Type</th><th>WRB</th><th>Description</th></tr>
<tr><td>H</td><td>L</td><td>8080 series</td><td>RDB</td><td>Read enable clock input pin.
When RDB is “L”, DB[15:0] are in an
output status.</td></tr>
<tr><td>H</td><td>H</td><td>6800 series</td><td>E</td><td>Read / Write control input pin.
-R/W = “H” : When E is “H”, DB[15:0] are in
an output status.
-R/W = “L” : The data on DB[15:0] are latched
at the falling edge of the E signal.</td></tr>
</table></td></tr>
</table>

MPU Interface Pins *(Continued)*

PIN	NAME	I/O	Description
	DB[15:8] DB[7]/SDI DB[6]/SCL DB[5:0]	I / O	-DB[15:0] : 16bit bi-directional data bus. Used as MSB 8bit data bus(D15~D8) in the 16bit data RAM transfer mode. When 8bit data bus is used, D15~D8 is set to “L” or “H”. -SDI : Serial data input pin. The data is latched at the rising edge of the SCL. -SCL : Serial clock input pin. Set to “L” after data transfer.
	CDIR	I	Common direction select pin. Fix to “L or H”

8.3 Oscillator and analog Pins

PIN	NAME	I/O	Description
	EXMCLK	I	External main clock input pin. When Internal oscillator is used, EXMCLK pin is “L or H”.
	EXDCCLK	I	External dcdc clock input pin. When Internal dcdc oscillator is used, EXDCCLK pin is “L or H”.
	EXVREF	I	External reference voltage input pin. When Internal reference voltage is used, EXVREF pin is “open”.

8.4 LCD driver output Pins

PIN	NAME	I/O	Description
	SEGA0 ~ SEGA127	O	LCD driving segment outputs (Red or Blue).
	SEGB0 ~ SEGB127	O	LCD driving segment outputs (Green).
	SEGC0 ~ SEGC127	O	LCD driving segment outputs (Blue or Red).
	COM0 ~ COM159	O	LCD driving common outputs.

8.5 Test Pins

PIN	NAME	I/O	Description
	CLKO	O	Dummy pin for verification. Fix to “open”
	TRIMEN	I	Dummy pin for verification. Fix to “open”
	TRCON	I	Dummy pin for verification. Fix to “open”
	TSTO	O	Dummy pin for verification. Fix to “open”
	VREF0	O	Dummy pin for verification. Fix to “open”

9. FUNCTION DESCRIPTION

9.1 MPU Interface

Chip Selection Input

There are CS1B and CS2 pins for chip selection. The HDC1600 can interface with an MPU only when CS1B is “L” and CS2 is “H”. When these pins are set to any other combination, RS. RDB, and WRB inputs are disable and DB15 ~ DB0 are to be high impedance. And, in case of serial interface, the internal shift register and the counter are reset.

Parallel / Serial Interface

The HDC1600 has eight types of interface with an MPU, which are four serial and four parallel interfaces. The HDC1600 receives data through 8bit parallel I/O (DB7 ~ DB0), 16bit parallel I/O (DB15 ~ DB0) or divided into serial data input (DB7 / SDI). This parallel or serial interface is determined by PS pin as shown in Table1. Reading out from internal register or RAM is not possible at serial interface.

Table 1. Parallel / Serial Interface Mode

PS	MPU[1]	MPU[0]	CS1B	CS2	Description
H	L	L	CS1B	CS2	8080-series 8bit interface
		H			8080-series 16bit interface
	H	L			6800-series 8bit interface
		H			6800-series 16bit interface
L	L	L			3-line 8bit SPI (Write only)
		H			3-line 16bit SPI (Write only)
	H	L			4-line 8bit SPI (Write only)
		H			4-line 16bit SPI (Write only)

Parallel Interface (PS=“H”)

The 8bit/16bit bi-directional data bus is used in parallel interface. The type of MPU is selected by MPU[1] and the mode of data-bus is controlled by MPU[0] as shown in below. In accessing internal registers (RS = “L”), only DB[7:0] are valid.

Table 2. Microprocessor Selection for Parallel Interface

MPU[1]	MPU[0]	CS1B	CS2	RDB	WRB	Data Bus	Description
L	L	CS1B	CS2	RDB	WRB	DB[7:0]	8080-series 8bit interface
	H					DB[15:0]	8080-series 16bit interface
H	L	CS1B	CS2	E	R/W	DB[7:0]	6800-series 8bit interface
	H					DB[15:0]	6800-series 16bit interface

Table 3. Parallel Data Transfer

RS	6800-series		8080-series		Description
	RDB (E)	WRB (R/W)	RDB	WRB	
H	H	H	L	H	Read display data
H	H	L	H	L	Write display data
L	H	H	L	H	Read out internal status register
L	H	L	H	L	Write instruction data

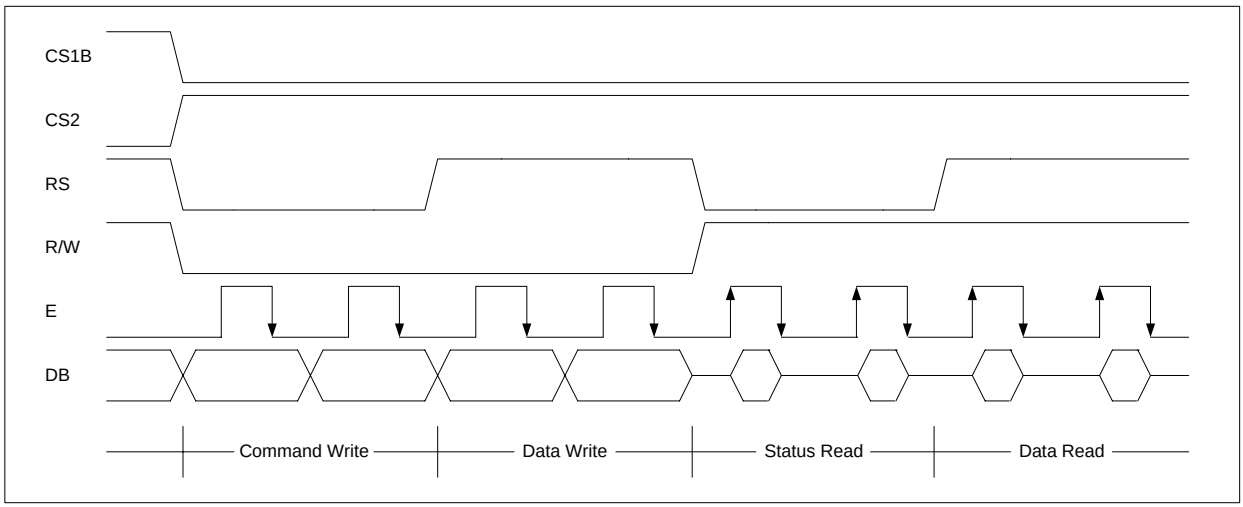


Figure 3. 6800-series MPU Interface protocol (MPU[1]="H")

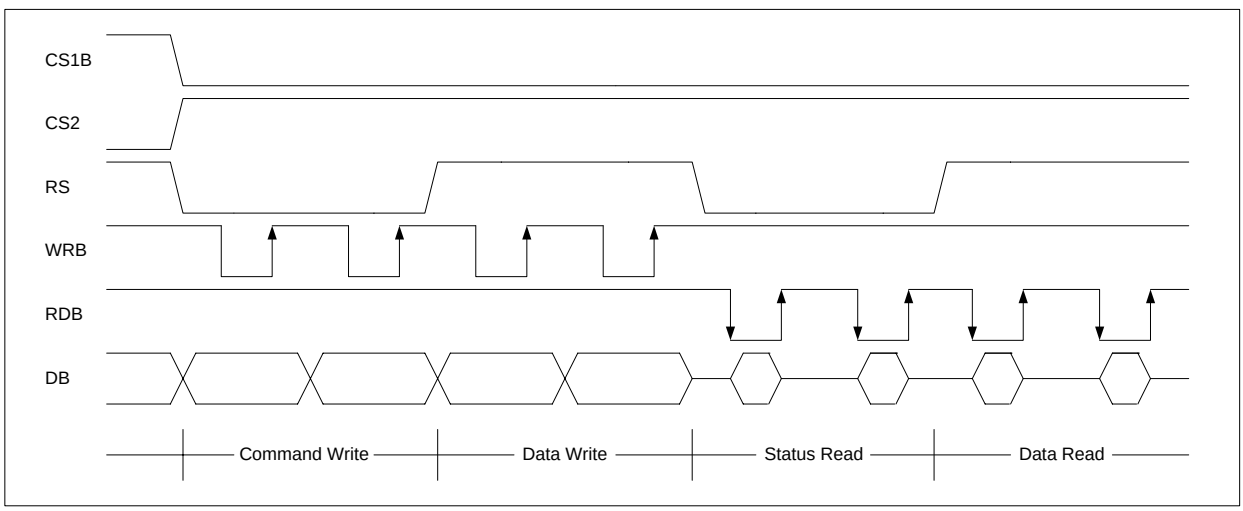


Figure 4. 8080-series MPU Interface protocol (MPU[1]="L")

Serial Interface (PS="L")

Communication with the microprocessor occurs via a clock-synchronized serial peripheral interface when PS is low. When using the serial interface, read operations are not allowed. When the chip select inputs are valid (CS1B = "L" & CS2 = "H"), the serial data is sent most significant bit first on the rising edge of a serial clock going into DB6 (SCL).

Table 4. Serial Interface Mode

PS	MPU[1]	MPU[0]	CS1B	CS2	Description
L	L	L	CS1B	CS2	3-line 8bit SPI (Write only)
		H			3-line 16bit SPI (Write only)
	H	L			4-line 8bit SPI (Write only)
		H			4-line 16bit SPI (Write only)

3-line Serial Interface

3-line serial interface by SDI and SCL is possible at chip selection state (CS1B = "L" & CS2 = "H"). When chip is not selected, internal shift register and counter are reset to initial value. Input data from SDI are latched at the rising edge of serial clock (SCL) in the sequence of RS, DB7 ~ DB0(DB15 ~ DB0) and converted to 8bit(16bit) parallel data and handled at the rising edge of 9th(17th) serial clock. Serial data (SDI) are identified to display data or instruction by RS data at the rising edge of first serial clock (SCL).

Table 5. 3-line Serial Interface RS Identification

RS	Description
L	Instruction
H	Display Data

Serial clock (SCL) should go to "L" at the non-access period and after 9bit (17bit) data transfer. SDI and SCL signals are sensitive to external noise. To prevent miss operation, chip selection state should be released (CS1B = "H" or CS2 = "L") after 9bit (17bit) data transfer as shown in the following Figure 5**.**

4-line Serial Interface

4-line serial interface by SDI and SCL is possible at chip selection state (CS1B="L" & CS2="H"). When chip is not selected, internal shift register and counter are reset to initial value. Serial input data from SDI are latched at the rising edge of serial clock (SCL) in the sequence of DB7 ~ DB0(DB15 ~ DB0) and converted into 8bit(16bit) parallel data at the rising edge of 8th(15th) serial clock. Serial data (SDI) are identified to display data or instruction by RS input signal.

Table 6. 4-line Serial Interface RS Identification

RS	Description
L	Instruction
H	Display Data

Make serial clock (SCL) "L" at the non-access period and after 8bit data transfer. SDI and SCL signals are sensitive to external noise. To prevent mal-function, chip selection state should be released (CS1B = "H" or CS2 = "L") after 8bit(16bit) data transfer as shown in the following Figure 6.

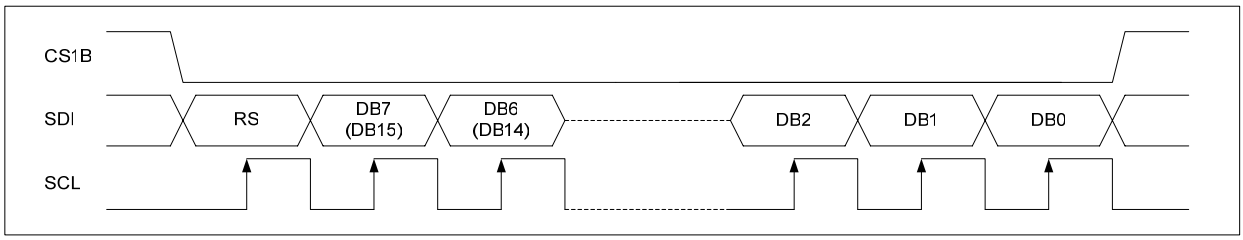


Figure 5. 3-line Serial Interface

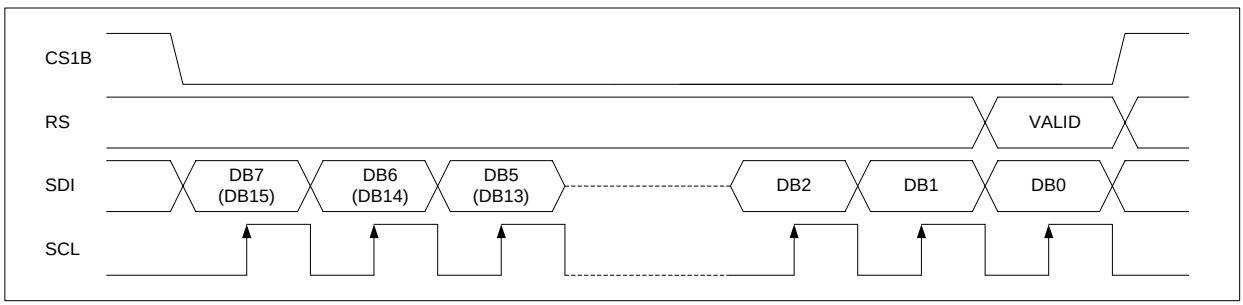


Figure 6. 4-line Serial Interface

Display RAM Access

Display RAM is accessed by data bus DB7~DB0(DB15~DB0), chip select pin (CS1B), display data/register select pin (RS), read/write control pin RDB or WRB pin. When CS1B="H", it is in non-selective state and display RAM access is impossible. During access, Set CS1B="L". Access selection to display RAM or internal register is controlled by RS port signal. Write process starts after setting address and then the data on the 8bit data bus or 16bit data bus, DB7 ~ DB0 / DB15 ~ DB0 will be written in by MPU. The data is written at the rising edge of WRB (8080-series) or falling edge of E (6800-series). Internally, bus holder data are processed to data bus and data are latched in bus holder until next cycle. There is a rule at reading out sequence of display RAM data. After setting address, data of assigned address are read at the 2nd clock of RDB, which means it, needs to read dummy data. In other words, 1 cycle dummy read operation is needed after address setting or writes cycle.

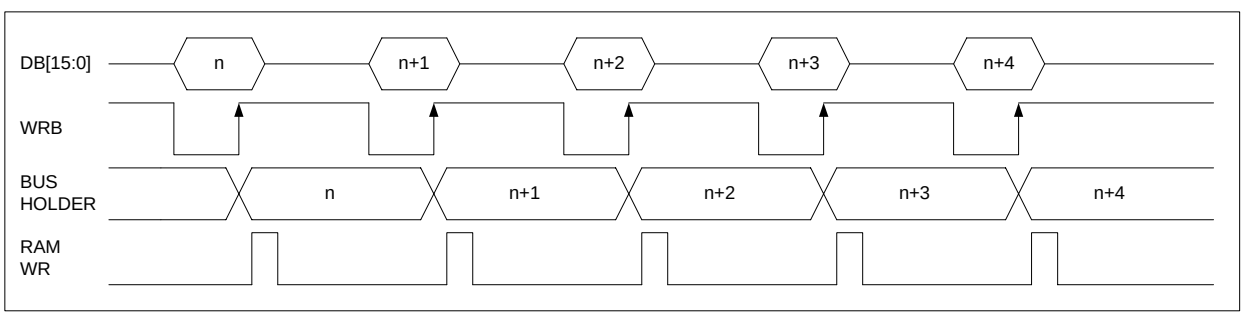


Figure 7. Data Write Operation

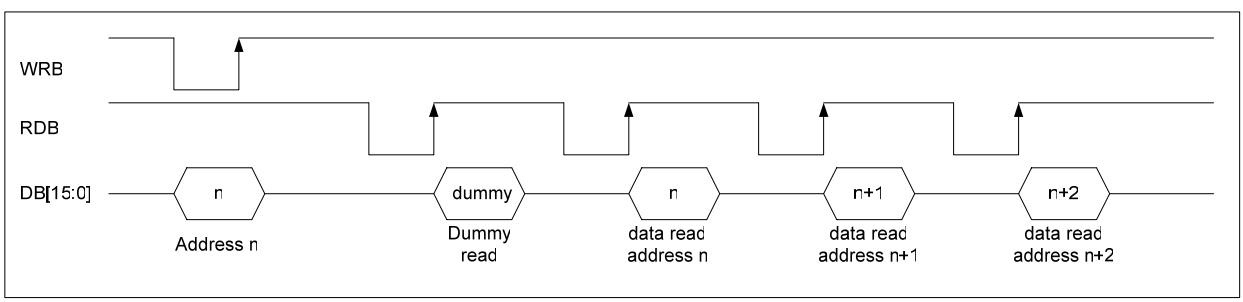


Figure 8. Data Read Operation

9.2 Display Data RAM

The on-chip display data RAM of HDC1600 is a static RAM that is stored the data for the display. It is a 128 x 160 x 16bits structure. It is controlled by 2 addresses, X and Y. And, RAM area selection and automatic address count up functions are accomplished by the internal instructions.

DDRAM Address Area Selection

A part of DDRAM address area of HDC1600 can be accessed by X and Y address area settings. After setting RAM area, the addresses become the start address.

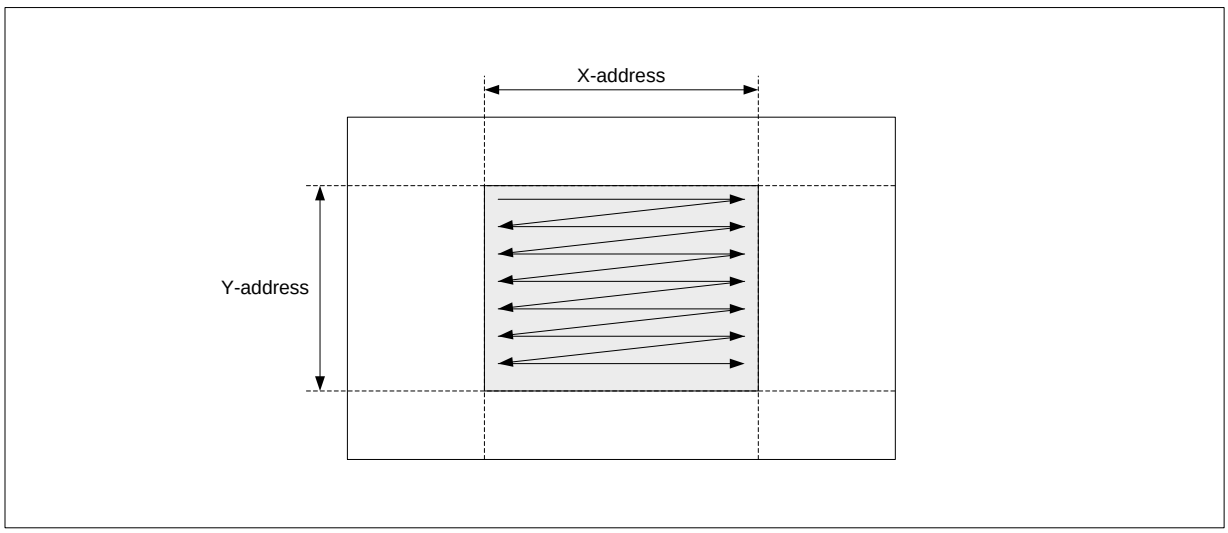


Figure 9. DDRAM Address Area

Table 7. X address Area Set

Code	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	0	1	0	0	0	0	1	1
P1	X start address set (Initial Status = 00H)							
P2	X end address set (Initial Status = 7FH)							

Table 8. Y address Area Set

Code	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	0	1	0	0	0	0	1	0
P1	Y start address set (Initial Status = 00H)							
P2	Y end address set (Initial Status = 9FH)							

RAM Addressing Count Up

By selecting the X address and Y address area by the internal instructions, the address counts up from its start address to end address after data access operation. When one address is equal to the end address, it returns to the start address. At this time, the other address is increased by 1.

X address count mode (X address = 00h ~ 7Fh, Y address = 00h ~ 9Fh)

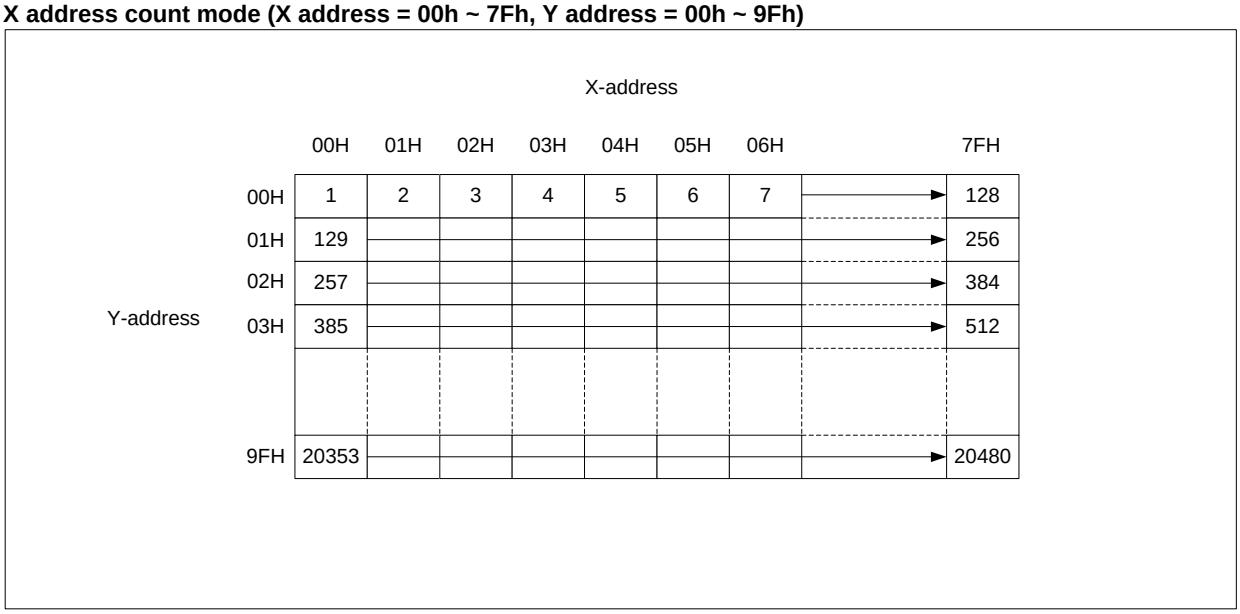


Figure 10. X Address Count Mode

Y address count mode (X address = 00h ~ 7Fh, Y address = 00h ~ 9Fh)

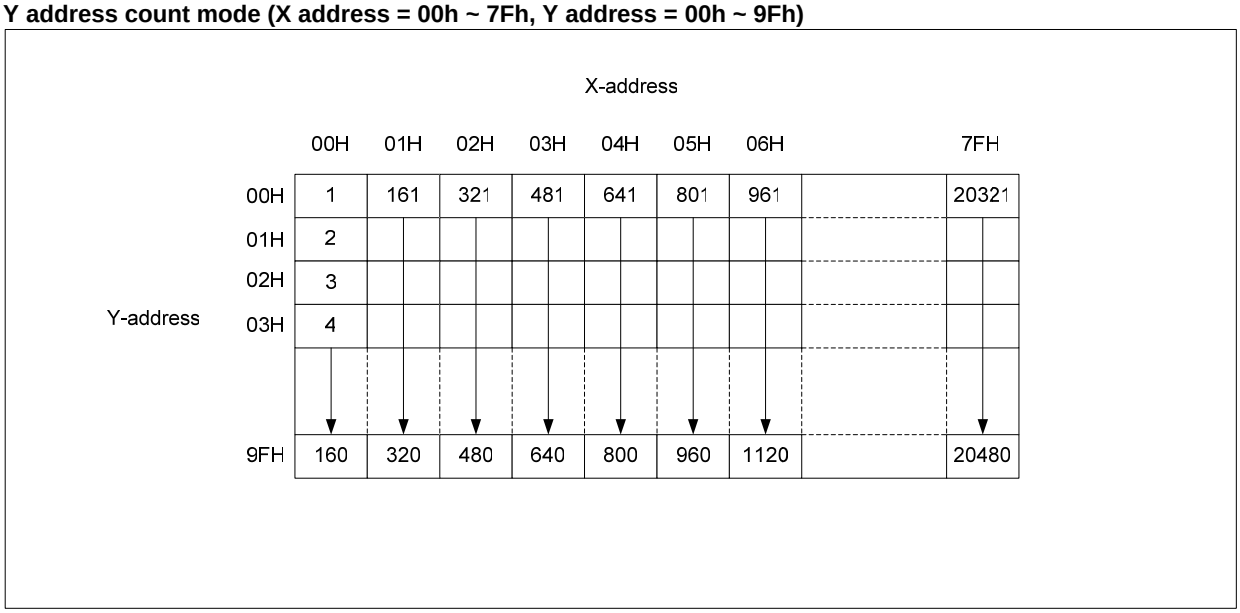


Figure 11. Y Address Count Mode

YA Address	XA Address															
	00H	01H	02H	03H	04H	05H	06H	07H	08H	----------	7AH	7BH	7CH	7DH	7EH	7FH
00H										----------						
01H										----------						
02H										----------						
03H										----------						
04H										----------						
05H										----------						
06H										----------						
07H										----------						
08H										----------						
09H										----------						
0AH										----------						
0BH										----------						
0CH										----------						
0DH										----------						
0EH										----------						
0FH										----------						
10H										----------						
⋮										⋮						
8FH										----------						
90H										----------						
91H										----------						
92H										----------						
93H										----------						
94H										----------						
95H										----------						
96H										----------						
97H										----------						
98H										----------						
99H										----------						
9AH										----------						
9BH										----------						
9CH										----------						
9DH										----------						
9EH										----------						
9FH										----------						

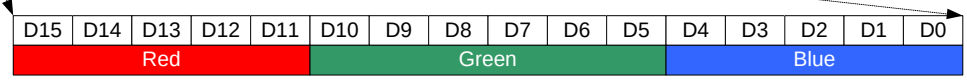


Figure 12. Display Data RAM Map

Partial Display Mode

The HDC1600 realizes the 1'st partial display and 2'nd partial display function with the various display duties. It is set as display start/end line number. Partial display can realize partial display at graphic display area on LCD panel. Partial display is used with lower duty than normal state at driving. And so, this operation can drive the LCD panel with lower bias ratio, lower boosting times and lower LCD driving voltages, and that can drive the LCD panel with lower power consumption. When using partial display function, the display duty can be selected by setting partial display end line set register. The display states such as LCD driving bias ratio, LCD driving voltage, electric volume setting value, boosting coefficient should be optimized to the selected LCD and display duty.

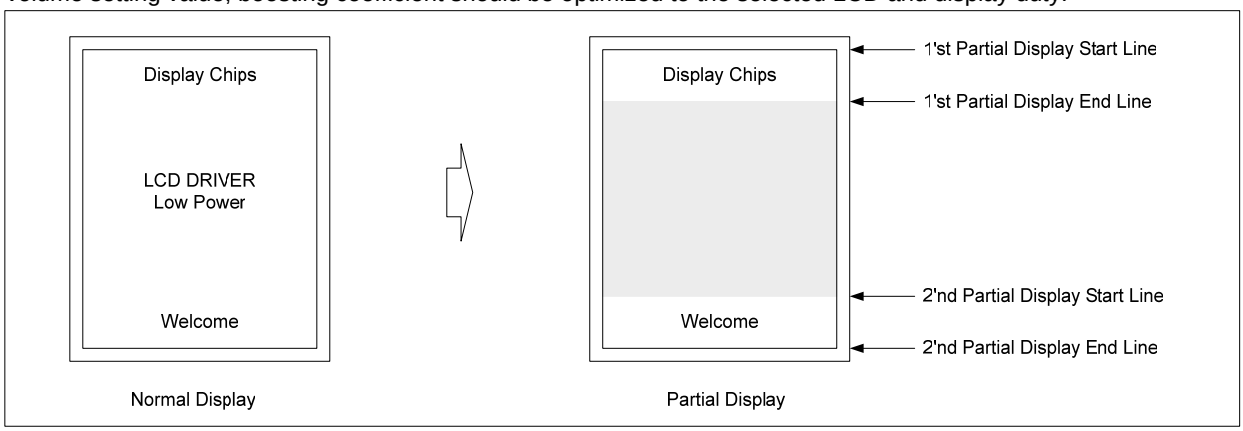


Figure 13. Partial Display Image

The next sequence should be followed carefully to realize partial display function.

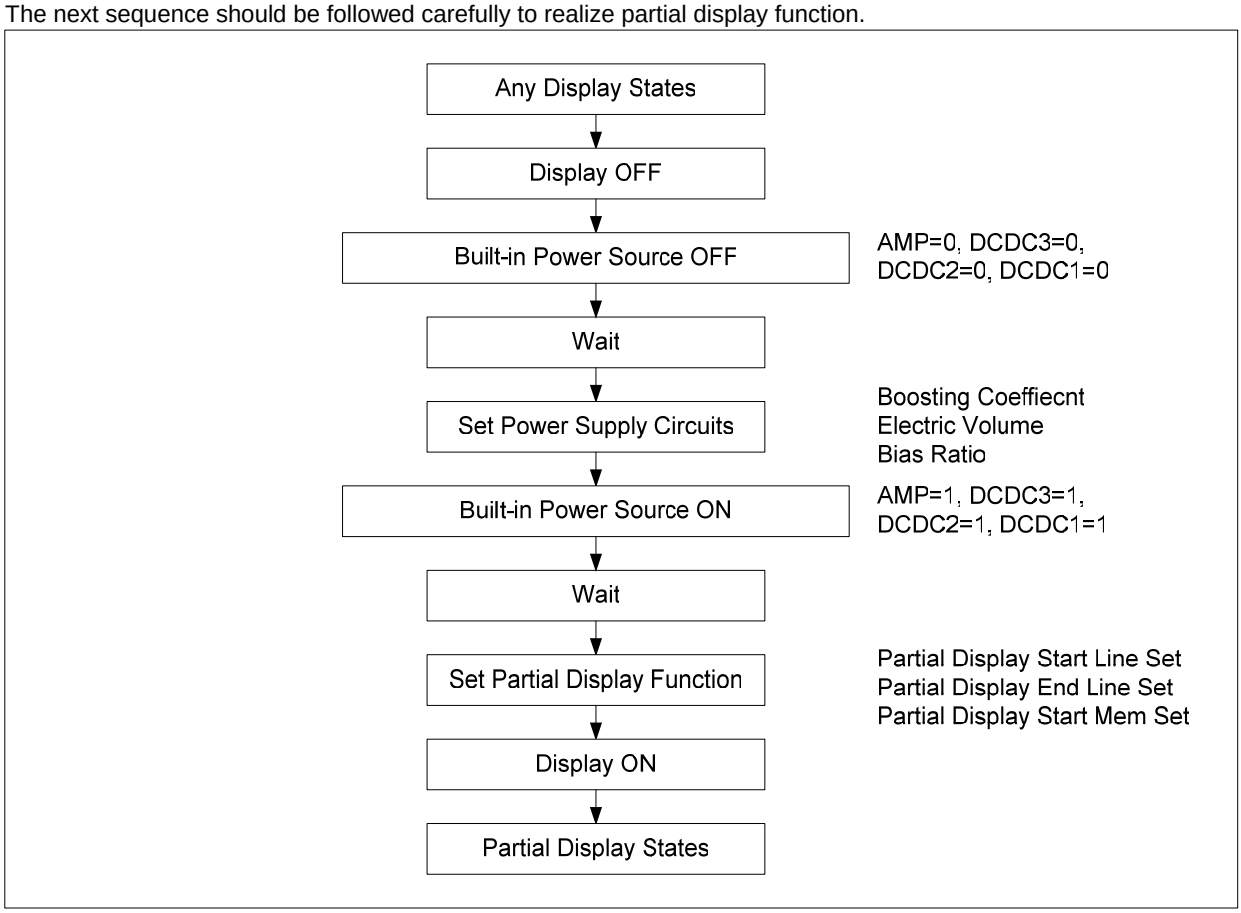


Figure 14. Partial Display Sequence

Display Direction

SDIR

The SDIR flag of Driver Output Mode Set instruction selects the direction of segment display.

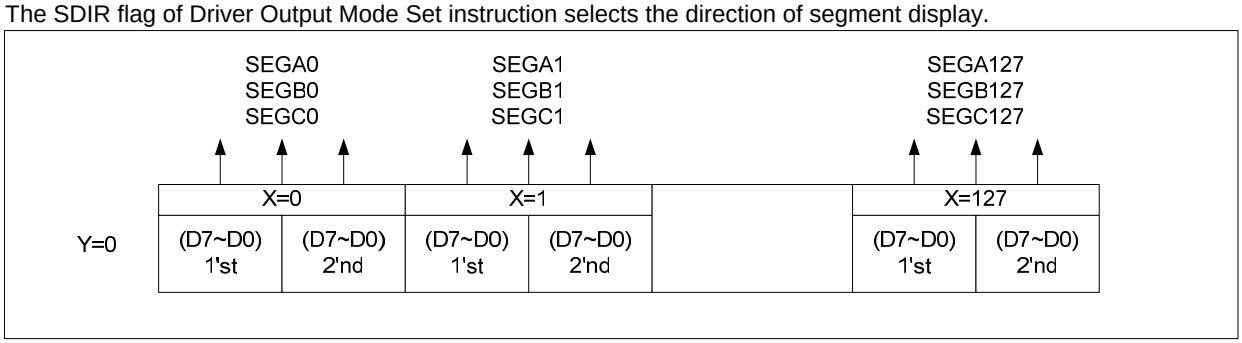


Figure 15. 8bit Data Bus Mode when SDIR = L

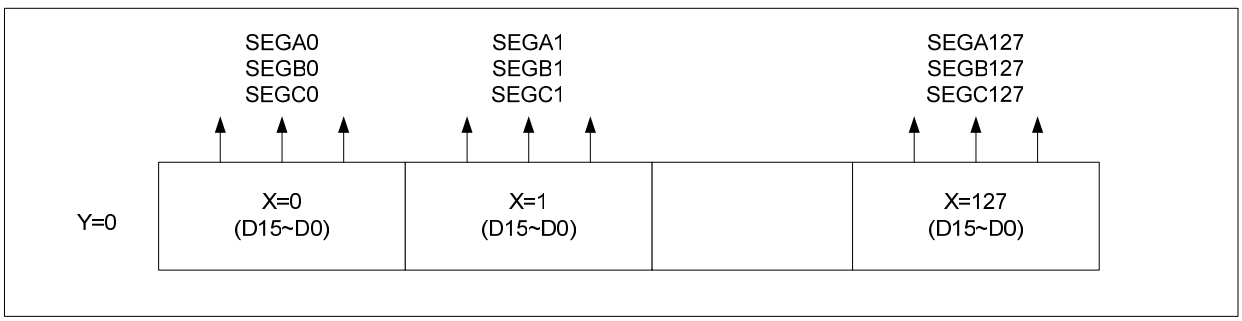


Figure 16. 16bit Data Bus Mode when SDIR = L

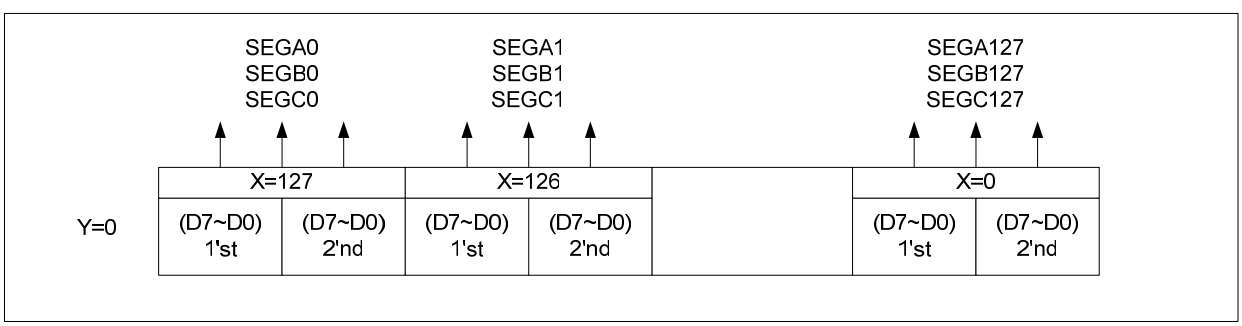


Figure 17. 8bit Data Bus Mode when SDIR = H

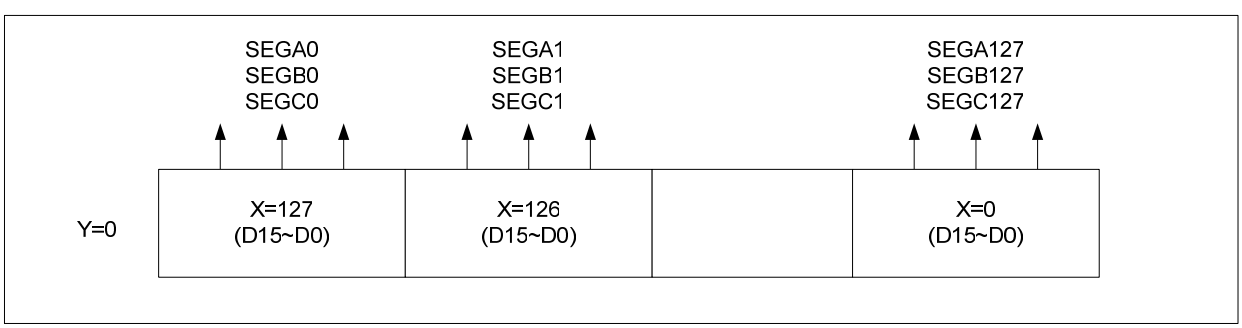


Figure 18. 16bit Data Bus Mode when SDIR = H

Next figure is DDRAM writing sequence with SDIR, Y address area.

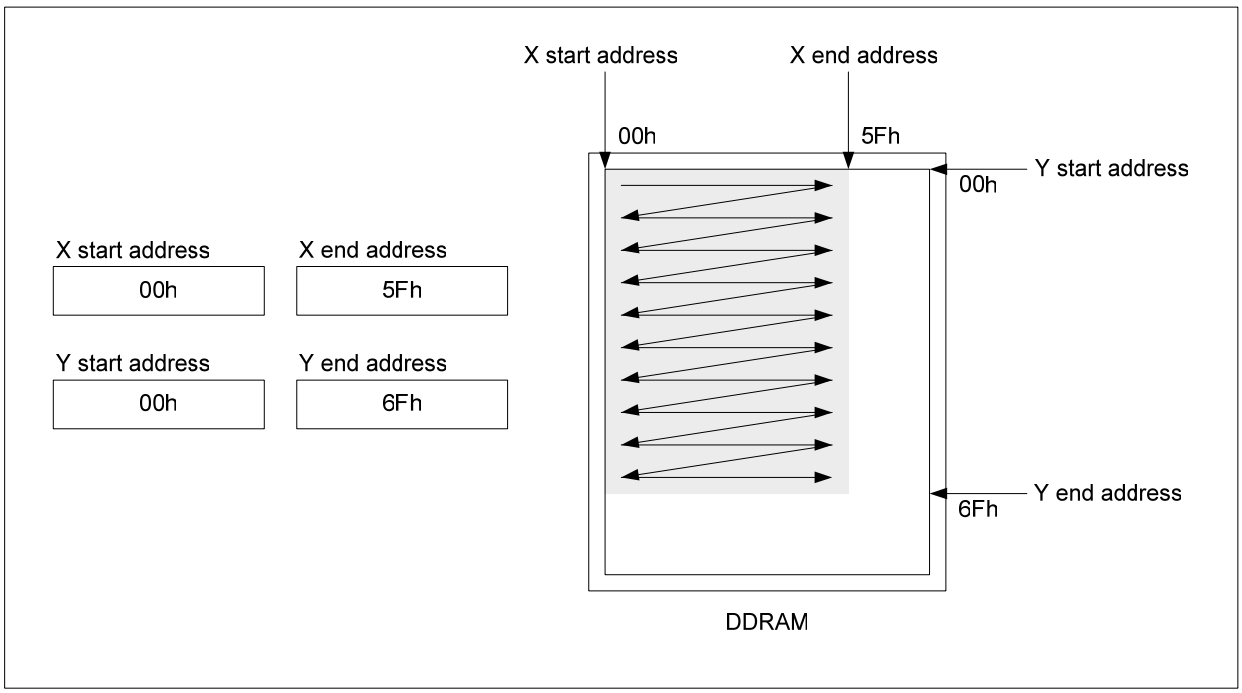


Figure 19. DDRAM Writing Sequence when SDIR = L

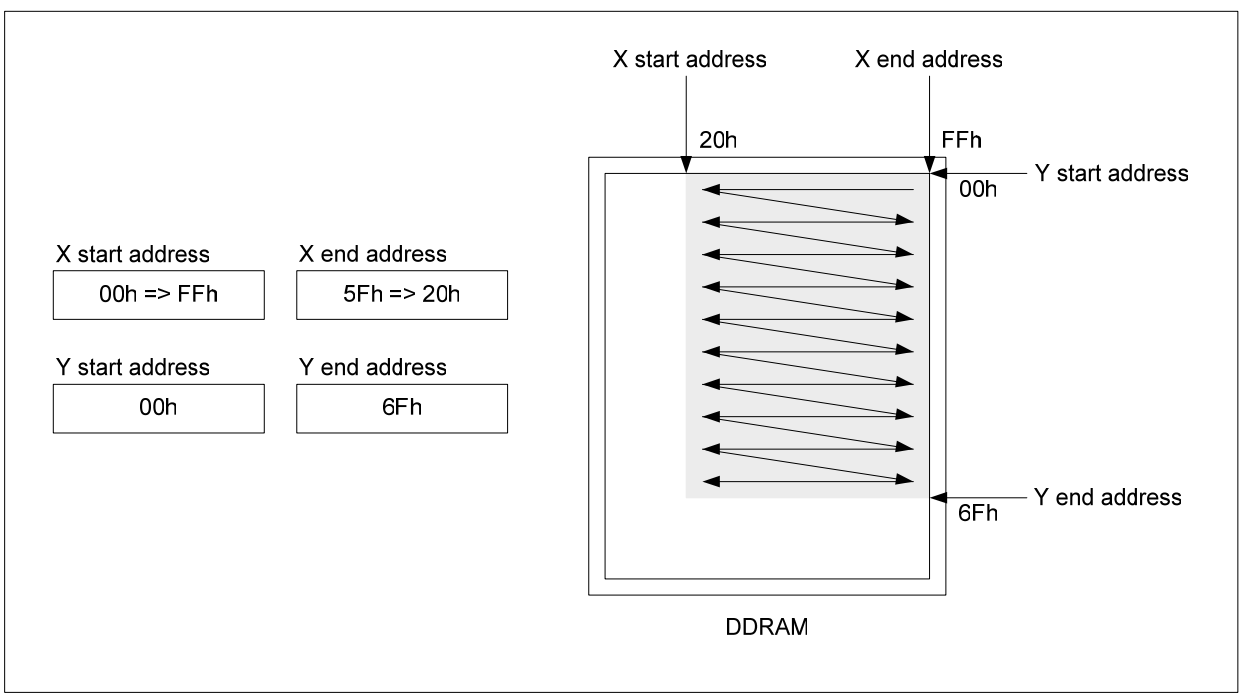
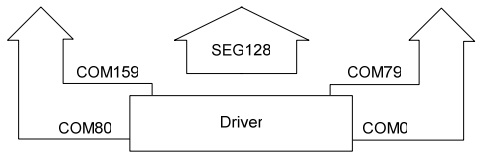


Figure 20. DDRAM Writing Sequence when SDIR = H

CDIR

The direction of common scanning is selected by CDIR pin.



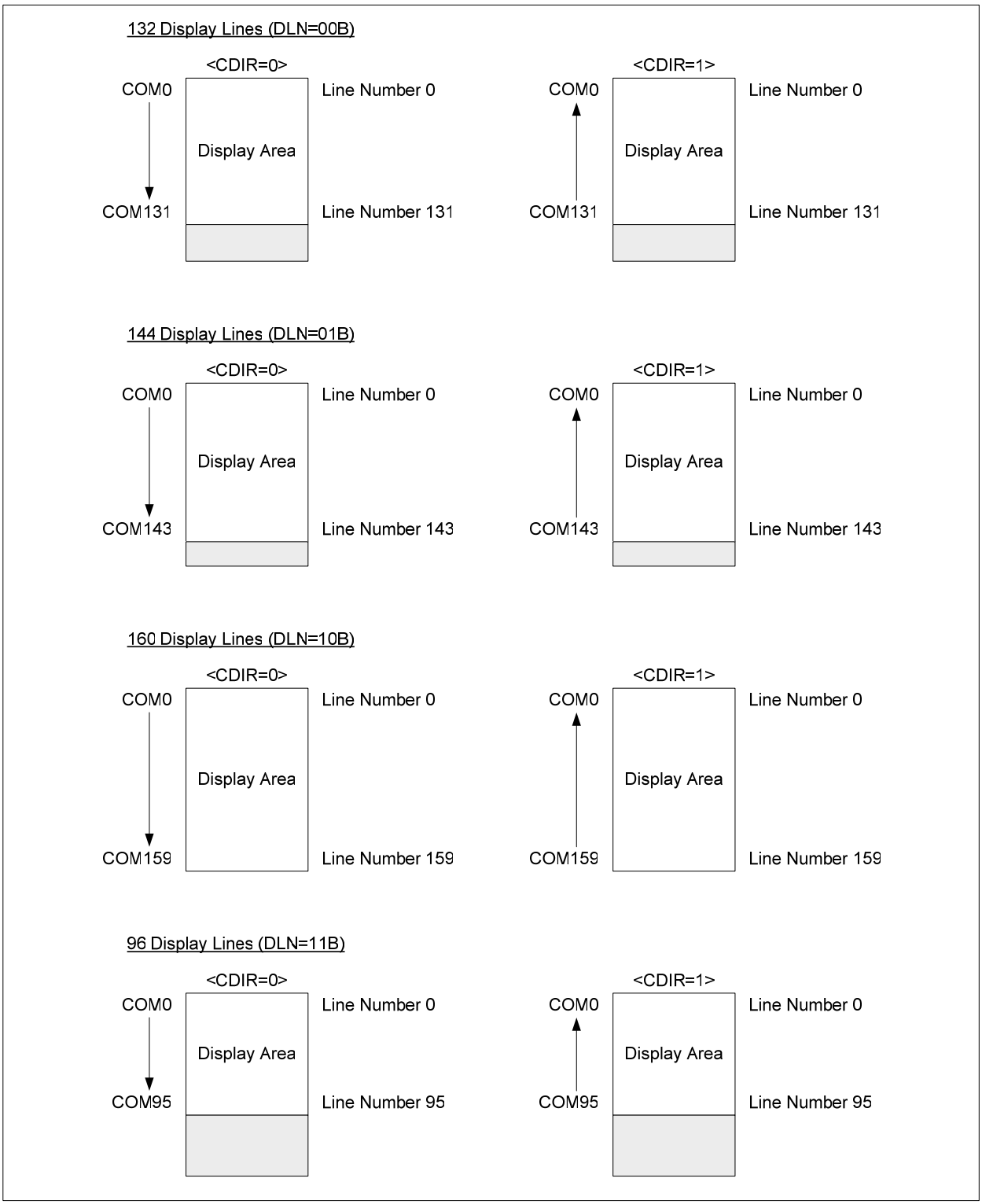
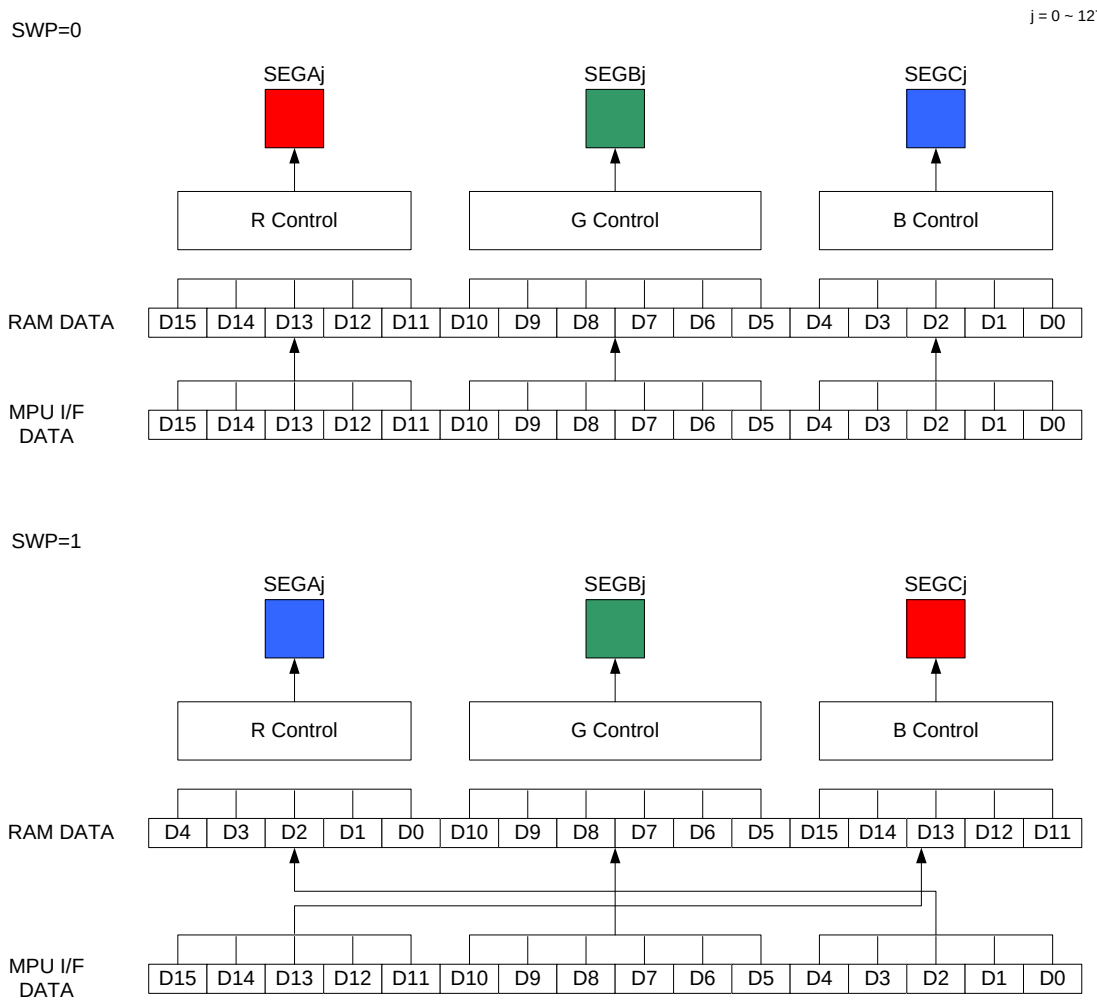


Figure 21. Direction by CDIR with DLN[1:0]

SWP

The SWP flag of Driver Output Mode Set instruction selects the swapping of segment display.



	SEGAj	SEGBj	SEGCj	
SWP=0	RED	GREEN	BLUE	Color
	D15~D11		D4~D0	Assigned Bit
SWP=1	BLUE	GREEN	RED	Color
	D4~D0	D10~D5	D15~D11	Assigned Bit

Figure 22. SEG outputs and RGB Color by SWP

HL

The HL flag of Entry Mode Set instruction selects the exchange higher and lower byte in 8bit data bus mode only for “Display Data Write/Read”.

8bit Interface Mode

HL=0

		X-address							
		00H		01H			9EH		7FH	
		MSB	LSB	MSB	LSB		MSB	LSB	MSB	LSB
Y-address	00H	1'st 8bit	2'nd 8bit	1'st 8bit	2'nd 8bit		1'st 8bit	2'nd 8bit	1'st 8bit	2'nd 8bit
	9FH	1'st 8bit	2'nd 8bit	1'st 8bit	2'nd 8bit		1'st 8bit	2'nd 8bit	1'st 8bit	2'nd 8bit

HL=1

		X-address							
		00H		01H			9EH		7FH	
		MSB	LSB	MSB	LSB		MSB	LSB	MSB	LSB
Y-address	00H	2'nd 8bit	1'st 8bit	2'nd 8bit	1'st 8bit		2'nd 8bit	1'st 8bit	2'nd 8bit	1'st 8bit
	9FH	2'nd 8bit	1'st 8bit	2'nd 8bit	1'st 8bit		2'nd 8bit	1'st 8bit	2'nd 8bit	1'st 8bit

16bit Interface Mode

HL=1 or 0

		X-address						
		00H		01H			9EH	7FH
		MSB	LSB	MSB	LSB		MSB LSB	MSB LSB
Y-address	00H	16bit		16bit			16bit	16bit
	9FH	16bit		16bit			16bit	16bit

Figure 23. Display RAM access by HL

9.3 Gradation Palette

The HDC1600 has 3 kinds of palette (palette Aj, palette Bj, palette Cj) with 128 gradation level. To implement 65K color display, R, B can be represented by selecting 32 gradation level among 128 gradation level and G is selecting 64 gradation level among 128 gradation levels.
To select the best suited gradation level for LCD panel at variable gradation display mode, please set 32 gradation register values among 128 gradation level. The PWM in according to the selected gradation is driven through segment driver outputs, SEGA(0~127), SEGB(0~127), and SEGC(0~127).

Table 9. Red / Blue Palette Gradation Table

RAM Data	Gradatiaon Level	Initial Value	RAM Data	Gradatiaon Level	Initial Value	RAM Data	Gradatiaon Level	Initial Value
00000	Level 0	0/127	01011	Level 11	50/127	10110	Level 22	83/127
00001	Level 1	10/127	01100	Level 12	53/127	10111	Level 23	86/127
00010	Level 2	18/127	01101	Level 13	56/127	11000	Level 24	89/127
00011	Level 3	24/127	01110	Level 14	59/127	11001	Level 25	92/127
00100	Level 4	28/127	01111	Level 15	62/127	11010	Level 26	95/127
00101	Level 5	32/127	10000	Level 16	65/127	11011	Level 27	99/127
00110	Level 6	35/127	10001	Level 17	68/127	11100	Level 28	103/127
00111	Level 7	38/127	10010	Level 18	71/127	11101	Level 29	109/127
01000	Level 8	41/127	10011	Level 19	74/127	11110	Level 30	117/127
01001	Level 9	44/127	10100	Level 20	77/127	11111	Level 31	127/127
01010	Level 10	47/127	10101	Level 21	80/127	-	-	-

Table 10. Green Palette Gradation Table

RAM Data	Gradatiaon Level	Initial Value	RAM Data	Gradatiaon Level	Initial Value	RAM Data	Gradatiaon Level	Initial Value
000000	Level 0	0/127	010110	Level 22	50/127	101100	Level 44	82/127
000001	Level 1	5/127	010111	Level 23	52/127	101101	Level 45	83/127
000010	Level 2	10/127	011000	Level 24	53/127	101110	Level 46	85/127
000011	Level 3	14/127	011001	Level 25	55/127	101111	Level 47	86/127
000100	Level 4	18/127	011010	Level 26	56/127	110000	Level 48	88/127
000101	Level 5	21/127	011011	Level 27	58/127	110001	Level 49	89/127
000110	Level 6	24/127	011100	Level 28	59/127	110010	Level 50	91/127
000111	Level 7	26/127	011101	Level 29	61/127	110011	Level 51	92/127
001000	Level 8	28/127	011110	Level 30	62/127	110100	Level 52	94/127
001001	Level 9	30/127	011111	Level 31	63/127	110101	Level 53	95/127
001010	Level 10	32/127	100000	Level 32	64/127	110110	Level 54	97/127
001011	Level 11	34/127	100001	Level 33	65/127	110111	Level 55	99/127
001100	Level 12	35/127	100010	Level 34	67/127	111000	Level 56	101/127
001101	Level 13	37/127	100011	Level 35	68/127	111001	Level 57	103/127
001110	Level 14	38/127	100100	Level 36	70/127	111010	Level 58	106/127
001111	Level 15	40/127	100101	Level 37	71/127	111011	Level 59	109/127
010000	Level 16	41/127	100110	Level 38	73/127	111100	Level 60	113/127
010001	Level 17	43/127	100111	Level 39	74/127	111101	Level 61	117/127
010010	Level 18	44/127	101000	Level 40	76/127	111110	Level 62	122/127
010011	Level 19	46/127	101001	Level 41	77/127	111111	Level 63	127/127
010100	Level 20	47/127	101010	Level 42	79/127	-	-	-
010101	Level 21	49/127	101011	Level 43	80/127	-	-	-

9.4 Display Control Circuits

Display Timing Generator

The display timing generator makes a timing clock and timing pulses for internal operation by input the external oscillator clock EXMCLK or by the internal oscillator circuit.

Signal Generator of Display Line Counter, Display Data Latch

The latch signal from line counter clock to display data latch circuit is generated from display clock. Synchronized with the display clock, the line addresses of Display RAM are generated and 2048 bit display data are latched to display data latching circuit and then output to the LCD driver circuit (SEG output port).
Read-out of the display data to the LCD drive circuit is completely independent of MPU side and so MPU can access it with no relationship with the read-out operation of the display data.

Generation of Display Timing Signal

The alternated internal signal (FRAME) and synchronous internal signal (CNOV) are generated from the display clock. Normally the alternated signal, FRAME is generated per frame. (inverse FRAME signal level per 1 frame) but, by setting up data (n-1) on n-line inversion register and “1” on n-line alternated instruction (NLION), n-line inverse waveform can be generated.

LCD Driver Circuit

This driver circuit generates four levels of LCD driver voltage. The circuit has 384 segment outputs, 160 common outputs and outputs combined display data and internal FRAME signal. The common driver circuit that has shift registers and outputs common scan signals sequentially.

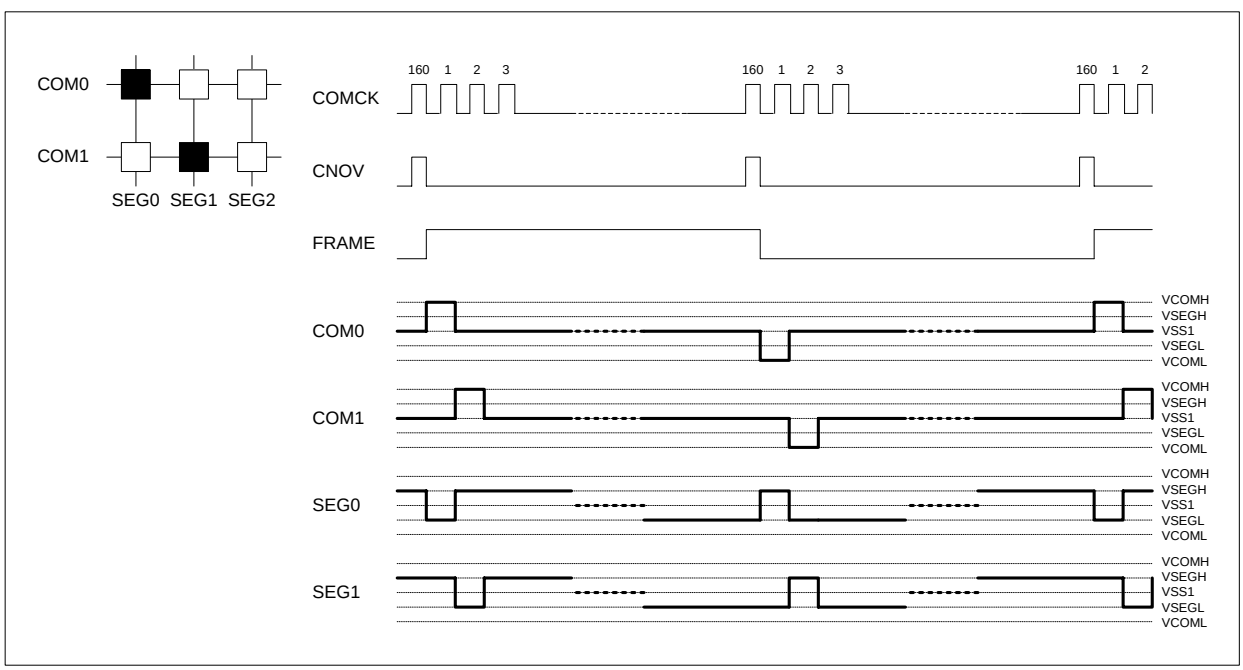


Figure 24. Waveform of LCD Driving

9.5 Analog Circuits

Oscillator Circuit

The HDC1600 has the 2 kinds of internal ring oscillator. The output of main oscillator is used ad the timing signal source of display. If external clock is used, force 50% duty clock as input clock through EXMCLK pin. DCDC oscillator is used as clock to booster. The frame frequency and boosting clock frequency can be changed by instruction.

Voltage Booster Circuit

The HDC1600 has 3 kinds of voltage booster that generates the voltages necessary for driving LCD panel. The first and second voltage booster generates VCOMH, VCOML that used as Common high and low voltage. VSEGH is output of amp by selecting 1 level of 256 steps electric volume. VSEGH used as Segment high voltage. The third voltage booster generates VSEGL that used as Segment low voltage.
Voltage boosting circuit can generates the 4 kinds of voltages (VCOMH, VCOML, VSEGH, VSEGL) for LCD driving using external capacitors. For large panel driving, it's preferable to use external voltage source rather than to use built-in power supply circuit for good image quality. When using external voltage source, disable the built-in power supply circuit (AMPON, DCDC3, DCDC2, DCDC1 = '0000', EXDC = '1'), supply the VCOMH, VCOML, VSEGH, VSEGL externally and open the C11P, C11N, C12P, C12N, C13P, C13N, C14P, C14N, C15P, C15N, C21P, C21N, C31P, C31N, C32P, C32N terminals.
By connecting capacitors between C11P and C11N, C12P and C12N, C13P and C13N, C14P and C14N, C15P and C15N, C21P and C21N, C31P and C31N, C32P and C32N, VCOMH and VSS3, VCOML and VSS3, VSEGH and VSS3, VSEGL and VSS3, boosted voltage can be generated through VCOMH, VCOML, VSEGL port. The boosting coefficient can be set by command and 2-times/ 3-times / 4-times/ 5-times/ 6-times.
Special care should be taken so that the voltage of VCOMH would not exceed 16V MAX. VCOMH voltage exceeding 16V can cause malfunction and reliability problem.

Electric Volume

The electric volume is adjusting VCOMH, VCOML, VSEGH, VSEGL level with command can control the brightness of LCD. The 4 kinds of driving voltage is generated by selecting 1 level within 256 step electric volume controlled levels by setting 8 bits electric volume register.

Reference Voltage Generation Circuit

The reference voltage generation circuit has temperature compensation function. The output of reference voltage generation circuit is used as input voltage of electric volume circuit to generate LCD driving voltage. The LCD driving voltages can be made by applying external reference voltage to reference voltage input terminal EXVREF.

10. INSTRUCTION DESCRIPTION

Instruction Name	RS	WRB	RDB	DB15 ~DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.	Parameter
Non Operation	0	0	1	*	0	0	0	0	0	0	0	0	00	-
Oscillation Mode Set	0	0	1	*	0	0	0	0	0	0	1	0	02	1 Byte
Driver Output Mode Set	0	0	1	*	0	0	0	1	0	0	0	0	10	1 Byte
Boosting Coefficient Set	0	0	1	*	0	0	1	0	0	0	1	0	22	1 Byte
DCDC Clock Frequency Set	0	0	1	*	0	0	1	0	0	1	0	0	24	1 Byte
DCDC and AMP ON/OFF Set	0	0	1	*	0	0	1	0	0	1	1	0	26	1 Byte
Temperature Compensation Set	0	0	1	*	0	0	1	0	1	0	0	0	28	1 Byte
Contrast Control(3) : EVOLC	0	0	1	*	0	0	1	0	1	0	0	1	29	1 Byte
Contrast Control(1) : EVOLS 1	0	0	1	*	0	0	1	0	1	0	1	0	2A	1 Byte
Contrast Control(2) : EVOLS 2	0	0	1	*	0	0	1	0	1	0	1	1	2B	1 Byte
Standby Mode ON/OFF	0	0	1	*	0	0	1	0	1	1	0	STB	2C/2D	-
DDRAM Burst Mode ON/OFF	0	0	1	*	0	0	1	0	1	1	1	BST	2E/2F	-
N-Line Inversion Set	0	0	1	*	0	0	1	1	0	1	0	0	34	1 Byte
Main Clock Frequency Set	0	0	1	*	0	0	1	1	0	1	1	0	36	1 Byte
Entry Mode Set	0	0	1	*	0	1	0	0	0	0	0	0	40	1 Byte
Y-address Area Set	0	0	1	*	0	1	0	0	0	0	1	0	42	2 Bytes
X-address Area Set	0	0	1	*	0	1	0	0	0	0	1	1	43	2 Bytes
Bias Set	0	0	1	*	0	1	0	0	0	1	1	0	46	1 Byte
Display ON/OFF	0	0	1	*	0	1	0	1	0	0	0	DISP	50/51	-
Specified Display Pattern Set	0	0	1	*	0	1	0	1	0	0	1	1	53	1 Byte
Partial Display Mode Set	0	0	1	*	0	1	0	1	0	1	0	1	55	1 Byte
Partial Display 1 Start Line Set	0	0	1	*	0	1	0	1	0	1	1	0	56	1 Byte
Partial Display 1 End Line Set	0	0	1	*	0	1	0	1	0	1	1	1	57	1 Byte
Partial Display 1 Start Memory Set	0	0	1	*	0	1	0	1	1	0	1	0	5A	1 Byte
MPE Mode ON/OFF	0	0	1	*	0	1	0	1	1	1	0	MPE	5C/5D	-
Partial Display 2 Start Line Set	0	0	1	*	0	1	1	0	0	0	0	0	60	1 Byte
Partial Display 2 End Line Set	0	0	1	*	0	1	1	0	0	0	1	0	62	1 Byte
Partial Display 2 Start Memory Set	0	0	1	*	0	1	1	0	0	1	0	0	64	1 Byte
Common Scan Mode Set	0	0	1	*	0	1	1	0	0	1	1	CMS	66/67	-
Y-address Decrement Set	0	0	1	*	0	1	1	0	1	0	0	YDE	68/69	-
Blank Time Set	0	0	1	*	0	1	1	0	1	0	1	0	6A	2 Bytes
Gradation Red Palette Set	0	0	1	*	0	1	1	1	0	0	0	0	70	32 Bytes
Gradation Green Palette Set	0	0	1	*	0	1	1	1	0	0	0	1	71	64 Bytes
Gradation Blue Palette Set	0	0	1	*	0	1	1	1	0	0	1	0	72	32 Bytes
Display Data Write	1	0	1	Write Display Data									-	-
Display Data Read	1	1	0	Read Display Data									-	-
Status Read	0	1	0	0	Status Data Read								-	-
User Trim Mode ON/OFF	0	0	1	*	1	1	1	0	1	0	1	UTE	EA/EB	-
User Trim/Reg Selection	0	0	1	*	1	1	1	0	1	1	0	0	EC	1 Byte
User EVOL Offset Volume Set	0	0	1	*	1	1	1	0	1	1	0	1	ED	1 Byte
User Trim Write Enable/Disable	0	0	1	*	1	1	1	0	1	1	1	UWT	EE/EF	-
Test Mode 1	0	0	1	*	0	1	0	1	1	1	1	0	5E	1 Byte
Test Mode 2	0	0	1	*	0	1	1	0	1	0	1	1	6D	-
Test Mode 3	0	0	1	*	0	1	1	0	1	1	1	1	6F	-
Test Mode 4	0	0	1	*	1	0	0	0	0	0	0	0	80	1 Byte
Test Mode 5	0	0	1	*	1	0	0	0	0	0	0	1	81	1 Byte
Test Mode 6	0	0	1	*	1	0	0	0	0	0	1	0	82	1 Byte
Test Mode 7	0	0	1	*	1	1	1	1	1	0	0	0	F8	1 Byte
Test Mode 8	0	0	1	*	1	1	1	1	1	0	0	1	F9	1 Byte
Test Mode 9	0	0	1	*	1	1	1	1	1	0	1	0	FA	1 Byte

notice 1) * mark is Don't care.

notice 2) Parameter : The number of parameter bytes that follows instruction data.

Non Operation

This instruction is non operation.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
0	0	1	0	0	0	0	0	0	0	0	00

Oscillation Mode Set

Setting internal / external main oscillator and dcdc oscillator mode.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
0	0	1	0	0	0	0	0	0	1	0	02
			0	0	0	0	EXTD	OSCDE	EXTM	OSCME	-

EXTD : external DCDC clock input selecting.
- EXTD = 0: Internal DCDC clock input (initial status).
- EXTD = 1: External DCDC clock input.

OSCDE : Internal DCDC oscillator ON/OFF.
- OSCDE = 0 : Internal DCDC oscillator OFF (initial status).
- OSCDE = 1 : internal DCDC oscillator ON.

EXTM : External main clock input selecting.
- EXTM = 0 : Internal main clock input (initial status).
- EXTM = 1 : External main clock input.

OSCME : Internal Main oscillator ON/OFF.
- OSCME = 0 : Internal oscillator OFF (initial status).
- OSCME = 1 : internal oscillator ON.

Driver Output Mode Set

This instruction sets the display direction and line.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
0	0	1	0	0	0	1	0	0	0	0	10
			0	0	DLN[1:0]		0	SDIR	SWP	0	-

DLN : Display line number selecting.

DLN[1:0]		Display Duty
0	0	1/132
0	1	1/144
1	0	1/160(initial status)
1	1	1/96

SDIR : Segment direction. This bits is for controlling the direction of segment driver.
- SDIR = 0 : writing display data from Y address 00H to 7FH (initial status).
- SDIR = 1 : writing display data from Y address 7FH to 00H.

SWP : Swap segment output SEGAj and SEGCj. This bit is for swapping the output of segment driver.
- SWP = 0 : normal state, D7~D0 or D15~D0 are written to the RAM as it is (initial status).
- SWP = 1 : swap mode ON state. The swapped data of D7~D0 or D15~D0 are written to the RAM.

Next figures are Waveform of LCD driving by DLN[1:0] value.

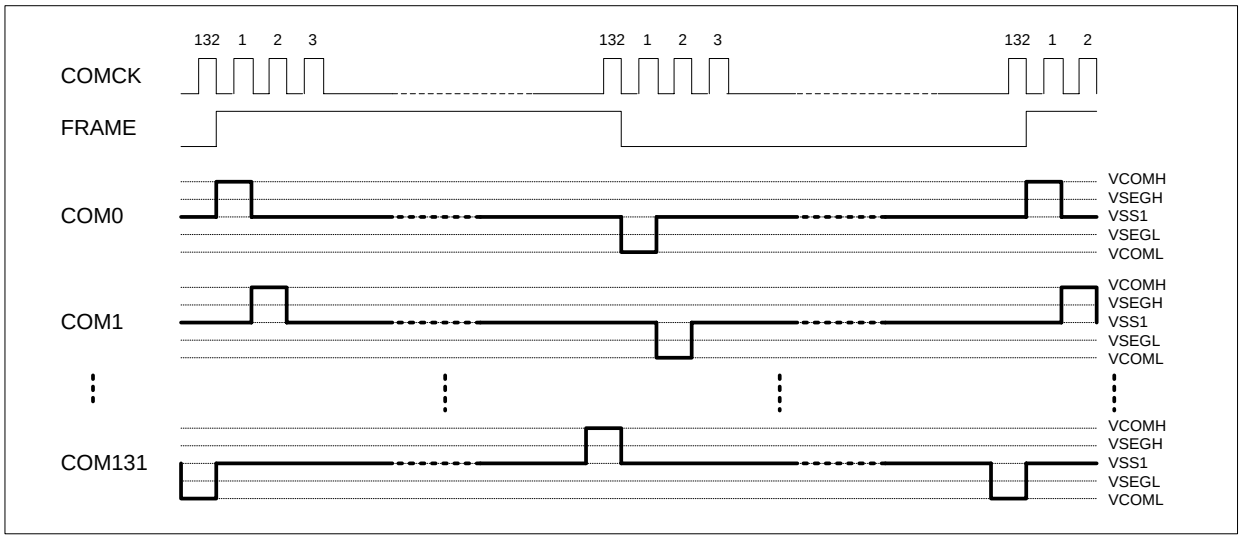


Figure 25. Waveform of LCD Driving DLN[1:0] = 2'b00

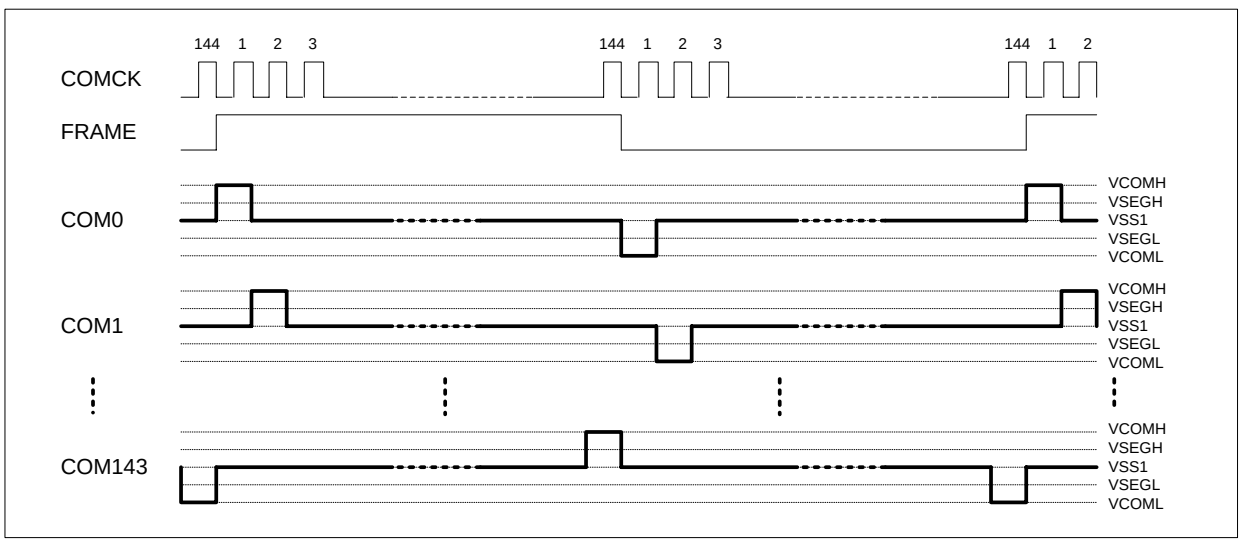


Figure 26. Waveform of LCD Driving DLN[1:0] = 2'b01

(Continued)

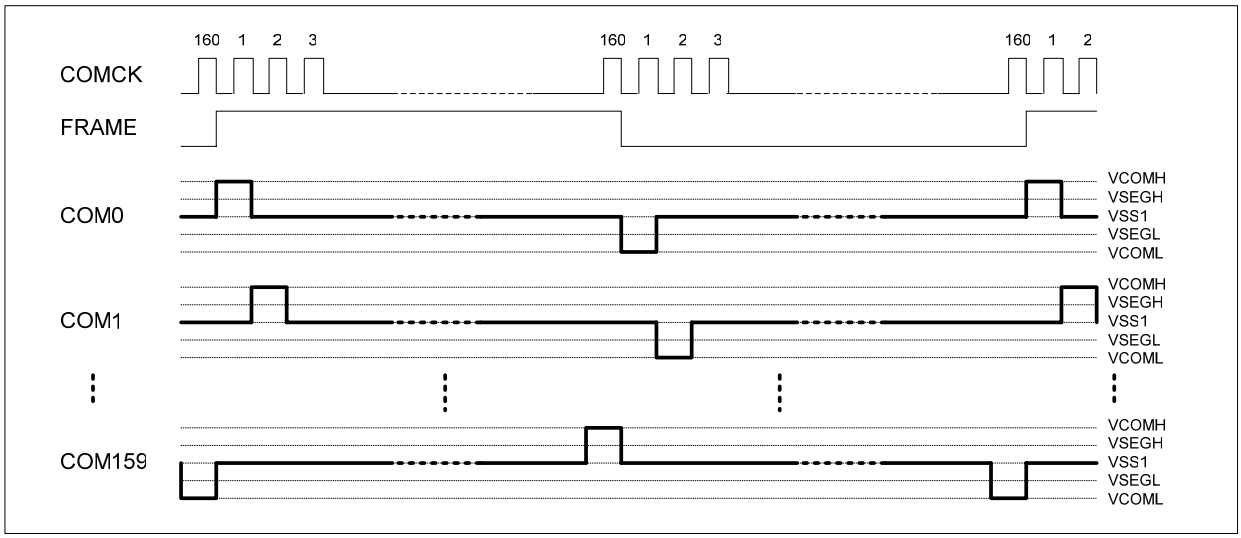


Figure 27. Waveform of LCD Driving DLN[1:0] = 2'b10

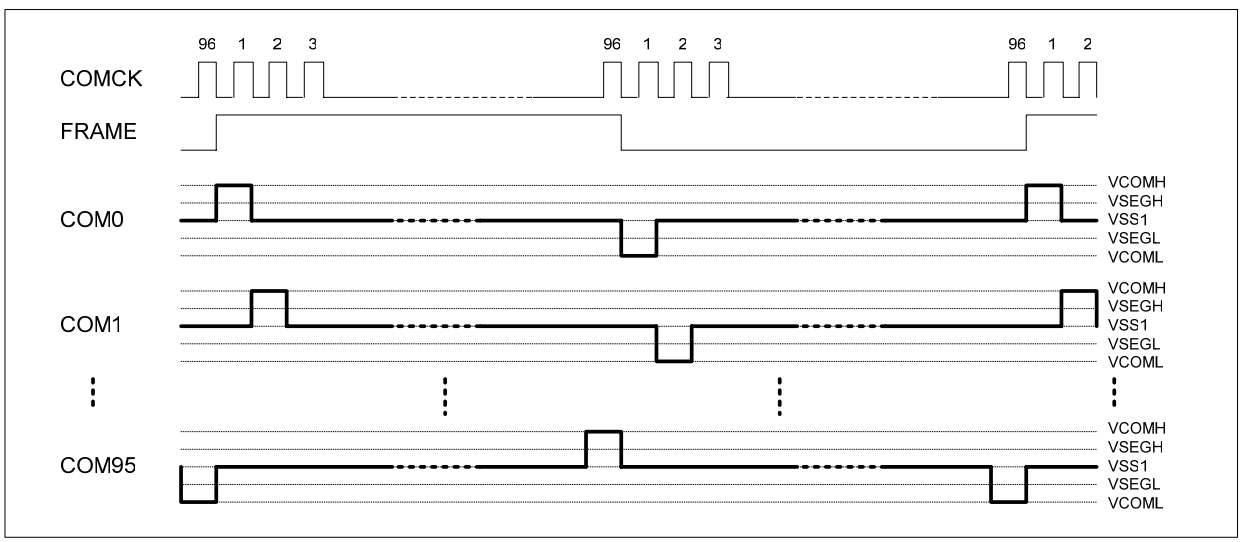


Figure 28. Waveform of LCD Driving DLN[1:0] = 2'b11

Boosting Coefficient Set

This instruction set up the VCOMH, VCOML boosting coefficient in normal mode and in partial mode.

DI	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
RS	0	1	0	0	1	0	0	0	1	0	22
			0	BC2[2:0]			0	BC1[2:0]			-

BC1 : Boosting coefficient in normal mode.
BC2 : Boosting coefficient in partial mode.

BC2 : In partial mode			
BC2[2:0]			Boosting Coefficient
0	0	0	2 Times Boosting
0	0	1	2 Times Boosting
0	1	0	2 Times Boosting
0	1	1	3 Times Boosting
1	0	0	4 Times Boosting
1	0	1	5 Times Boosting
1	1	0	6 Times Boosting
1	1	1	6 Times Boosting

BC1 : In normal mode			
BC1[2:0]			Boosting Coefficient
0	0	0	2 Times Boosting
0	0	1	2 Times Boosting
0	1	0	2 Times Boosting
0	1	1	3 Times Boosting
1	0	0	4 Times Boosting
1	0	1	5 Times Boosting
1	1	0	6 Times Boosting
1	1	1	6 Times Boosting

If Boosting Coefficient is changed, External capacitor connection remain unchanged.

DCDC Clock Frequency Set

This instruction sets the internal booster clock frequency.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
0	0	1	0	0	1	0	0	1	0	0	24
			0	DCK2[2:0]			0	DCK1[2:0]			-

DCK1 : Voltage booster clock frequency in normal mode.
DCK2 : Voltage booster clock frequency in partial mode.

DCK2 : In partial mode			
DCK2[2:0]			Voltage booster clock frequency
0	0	0	4.0 kHz
0	0	1	6.0 kHz
0	1	0	8.0 kHz
0	1	1	12.0 kHz
1	0	0	16.0 kHz
1	0	1	24.0 kHz
1	1	0	32.0 kHz
1	1	1	48.0 kHz

DCK1 : In normal mode			
DCK1[2:0]			Voltage booster clock frequency
0	0	0	4.0 kHz
0	0	1	6.0 kHz
0	1	0	8.0 kHz
0	1	1	12.0 kHz
1	0	0	16.0 kHz
1	0	1	24.0 kHz
1	1	0	32.0 kHz
1	1	1	48.0 kHz

(*1) DCDC clock frequency tolerance is specified in DC characteristics1.

DCDC and AMP ON/OFF Set

This instruction set up the DC/DC and Op-amp in common start up setting.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
0	0	1	0	0	1	0	0	1	1	0	26
			EXDC	0	0	0	AMPON	DCDC3	DCDC2	DCDC1	-

EXDC : Internal / External LCD power select.
- EXDC = 0 : Internal DCDC power circuit (initial status).
- EXDC = 1 : External DCDC power circuit.

AMPON : Internal VSEGH Op-amp. ON/OFF.
- AMPON = 0 : Internal VSEGH power circuit OP-Amp. OFF (initial status).
- AMPON = 1 : Internal VSEGH power circuit OP-Amp. ON.

DCDC1 : 1'st voltage boosting circuit ON/OFF.
- DCDC1 = 0 : 1'st voltage boosting circuit OFF (initial status).
- DCDC1 = 1 : 1'st voltage boosting circuit ON.

DCDC2 : 2'nd voltage boosting circuit ON/OFF.
- DCDC2 = 0 : 2'nd voltage boosting circuit OFF (initial status).
- DCDC2 = 1 : 2'nd voltage boosting circuit ON.

DCDC3 : 3'rd voltage boosting circuit ON/OFF.
- DCDC3 = 0 : 3'rd voltage boosting circuit OFF (initial status).
- DCDC3 = 1 : 3'rd voltage boosting circuit ON.

Temperature Compensation Set

This Instruction sets up the driving voltage slope for temperature compensation.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
0	0	1	0	0	1	0	1	0	0	0	28
			0	0	0	0	0	TCS[2:0]			-

TCS : Temperature compensation slope set.

TCS[2:0]			Temperature coefficient ratio
0	0	0	0.00%/degC(initial status)
0	0	1	-0.05%/degC
0	1	0	-0.10%/degC
0	1	1	-0.15%/degC
1	0	0	-0.20%/degC
1	0	1	External reference voltage
1	1	0	
1	1	1	

Contrast Control(3) : EVOLC

This instruction set up common contrast by addition or subtraction from segment contrast.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
0	0	1	0	0	1	0	1	0	0	1	29
			0	0	Contrast3[5:0]						-

Common contrast control

CONTRAST3[5:0]						Common Contrast
0	0	0	0	0	0	Common Contrast Control. - CONTRAST3[5] = 0 : Common Contrast (EVOLC) = Segment Contrast[7:0] + CONTRAST3[4:0] - CONTRAST3[5] = 1 : Common Contrast (EVOLC) = Segment Contrast[7:0] – CONTRAST3[4:0]
0	0	0	0	0	1	
…….						
1	1	1	1	1	0	
1	1	1	1	1	1	

Contrast Control(1) : EVOLS 1

This instruction updates the segment contrast control value in normal display mode.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
0	0	1	0	0	1	0	1	0	1	0	2A
			Contrast1[7:0]								-

Segment contrast control in normal display mode.(3.0㎷ Step)

CONTRAST1[7:0]								Segment Contrast 1 (EVOLS 1)
0	0	0	0	0	0	0	0	1.035V(Low)
0	0	0	0	0	0	0	1	1.038V
⋮								⋮
1	1	1	1	1	1	1	0	1.797V
1	1	1	1	1	1	1	1	1.800V(High)

Contrast Control(2) : EVOLS 2

This instruction updates the segment contrast control value in partial display mode.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
0	0	1	0	0	1	0	1	0	1	1	2B
			Contrast2[7:0]								-

Segment contrast control in partial display mode.(3.0㎷ Step)

CONTRAST2[7:0]								Segment Contrast 2 (EVOLS 2)
0	0	0	0	0	0	0	0	1.035V(Low)
0	0	0	0	0	0	0	1	1.038V
⋮								⋮
1	1	1	1	1	1	1	0	1.797V
1	1	1	1	1	1	1	1	1.800V(High)

Next figures are LCD driving voltage by temperature coefficient (TCS[2:0]). and, block diagram of relation of EVOLS, EVOLC, User Trim cell. If EVOLS<7:0>=F0h and User Trim Cell<5:0>=1Fh, MEVOLS is 10FH, but MEVOLS<7:0> saturate at maximum value FFh. If EVOLS<7:0>=10h and User Trim Cell<5:0>=3Fh, MEVOLS<8:0> = -0Fh, but MEVOLS<7:0> stop at minimum value 00h. EVOLC<5:0> is same algorithm.

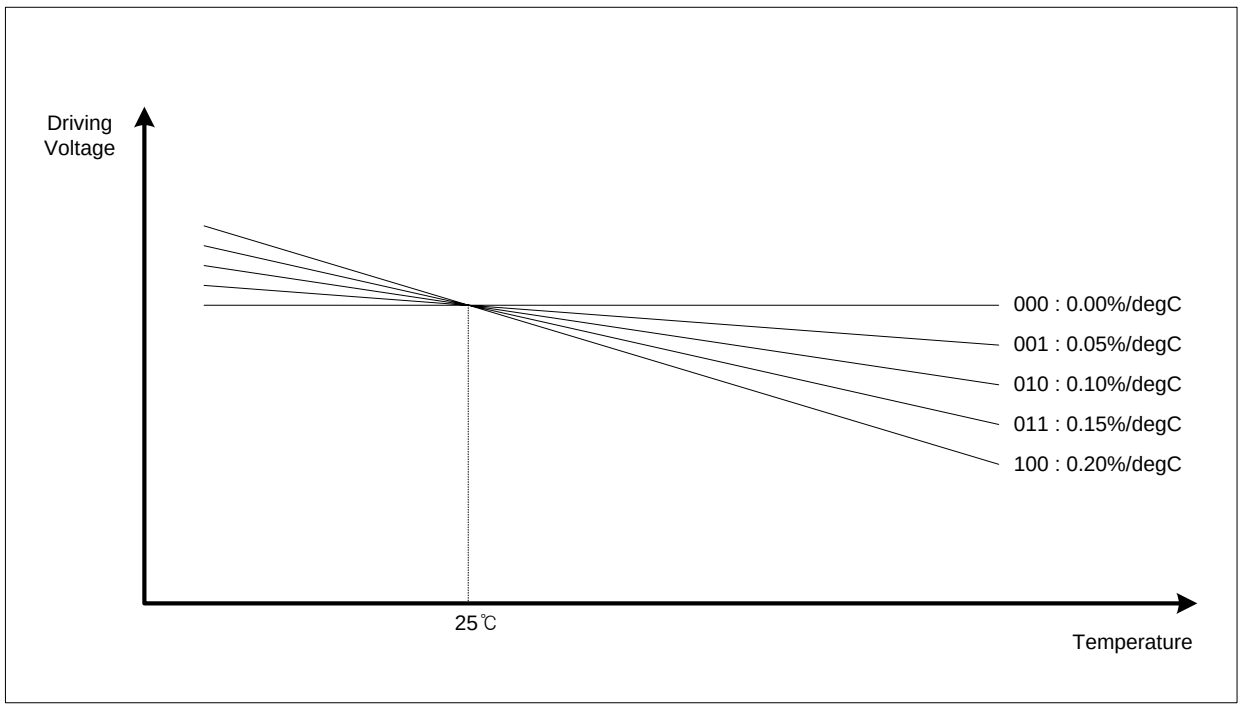


Figure 29. Temperature Coefficient by TCS[2:0]

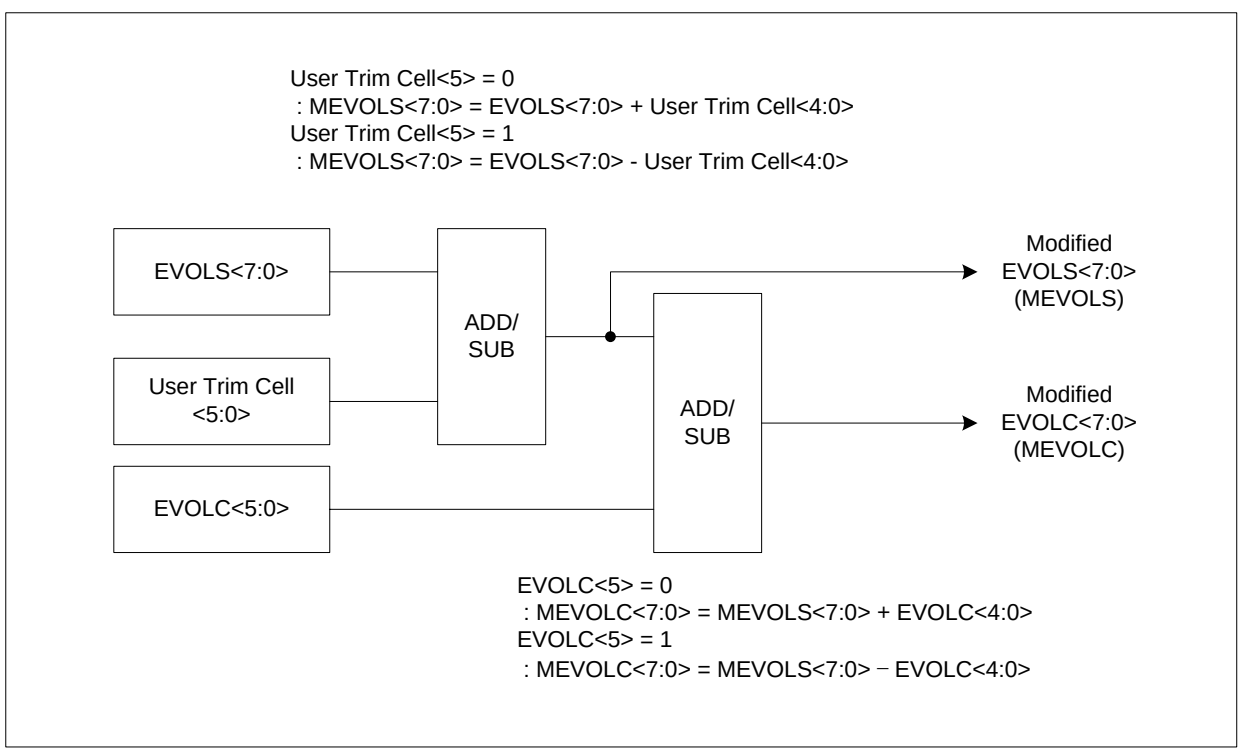


Figure 30. Relation of EVOLS, EVOLC, User Trim

Standby Mode ON/OFF

This instruction enter/releases the standby mode.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
0	0	1	0	0	1	0	1	1	0	STB	2C/2D

This instruction enters the standby mode to reduce the power consumption to the static power consumption value (initial status). The following instructions, standby off and display on, cause returning to the normal operation status.

- STB = 0 : Standby mode OFF.
- STB = 1 : Standby mode ON (Initial status).

The internal status during standby on are as following :

- All common and segment output : VSS1
- Oscillator circuit, built-in voltage booster block stop
- Clock input from EXMCLK port is disable
- Display RAM data are conserved
- Operational modes are preserved as those before standby mode ON instruction was executed
- VCOMH, VCOML, VSEGH, VSEGL become VSS1 state (EXDC = 0)

Make display off-state before power save mode by standby mode ON instruction.

DDRAM Burst Mode ON/OFF

This instruction set up DDRAM burst mode.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
0	0	1	0	0	1	0	1	1	1	BST	2E/2F

BST : Burst mode makes DDRAM current consumption minimize.

- BST = 0 : Burst mode OFF (initial status).
- BST = 1 : Burst mode ON.

N-line Inversion Set

This instruction set up N line inversion for AC driving.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
0	0	1	0	0	1	1	0	1	0	0	34
			NLION	NLI[6:0]							-

NLION : N-line inversion ON/OFF.

- NLION = 0 : N-line inversion OFF. Polarity signal, frame is inverted every other frame (initial status).
- NLION = 1 : N-line inversion ON. The n lines are inverted according to the contents of NLI[6:0].

NLI[6:0] indicates the period of polarity inversion.

NLI[6:0]							Inversion Line Number
0	0	0	0	0	0	0	Forbidden
0	0	0	0	0	0	1	3
0	0	0	0	0	1	0	5
⋮							⋮
1	0	0	1	1	1	0	157
1	0	0	1	1	1	1	159

Next figure is LCD driving waveform of N-Line inversion operation.

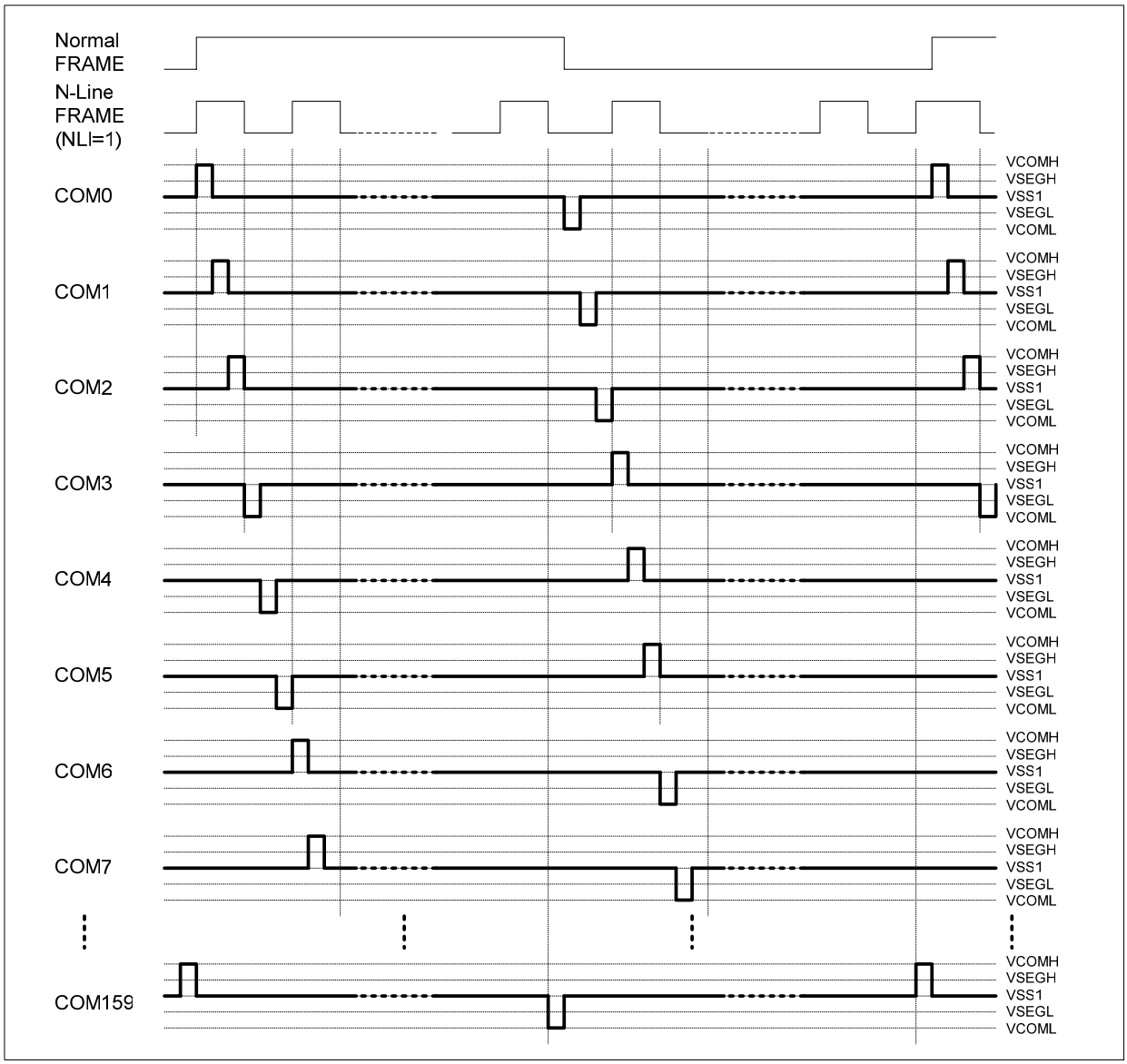


Figure 31. Waveform of N-Line Inversion LCD Driving (NLION=1, NLI[6:0] = 7'b0000001)

Main Clock Frequency Set

This instruction control the reference frequency of main oscillator circuit and the output frequency of divider. The frame frequency is changed according to the frequency of oscillator and the number of frequency divider. When you set the frame rate, please check the state of LCD display quality.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
0	0	1	0	0	1	1	0	1	1	0	36
			MDIV[1:0]		MCLK[5:0]						-

MDIV[1:0] : Main oscillator clock division.

MDIV[1:0]		COMCLK
0	0	MCLK
0	1	MCLK/2
1	0	MCLK/4
1	1	MCLK/8

(*1) Main clock frequency tolerance is specified in DC characteristics1.

MCLK[5:0] : Main oscillator frequency selection (25㎑ Step).

MCLK[5:0]						Main Oscillator Frequency
0	0	0	0	0	1	1.225㎒(Low)
0	0	0	0	1	0	1.250㎒
			⋮			⋮
0	1	1	1	1	1	1.975㎒
0(1)	0	0	0	0	0	2.000㎒
1	0	0	0	0	1	2.025㎒
			⋮			⋮
1	1	1	1	1	0	2.750㎒
1	1	1	1	1	1	2.775㎒(High)

Entry Mode Set

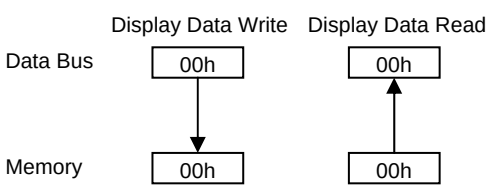
Setting internal function mode.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
0	0	1	0	1	0	0	0	0	0	0	40
			0	0	0	0	HL	MDI	X/Y	RMW	-

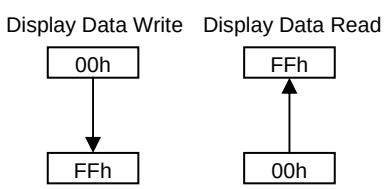
HL : Exchange higher and lower byte in 8-bit data bus mode only for “Display Data Write/Read”.
- HL = 0 : 8bit MSB(1’st data), 8bit LSB(2’nd data) (initial status).
- HL = 1 : 8bit LSB(1’st data), 8bit MSB(2’nd data).

MDI : Memory data inversion setting for low power consumption.
- MDI = 0 : Memory data inversion off (initial status).
- MDI = 1 : Memory data inversion on.

<MDI = 0>



<MDI = 1>



X/Y : Memory address counter mode setting.
- X/Y = 0 : X address count mode operation (initial status).
- X/Y = 1 : Y address count mode operation.

RMW : Read modify write mode ON/OFF select.
- RMW= 0 : Automatically increasing address at both case of writing in and read out display RAM data (initial status).
- RMW= 1 : Only when writing in display RAM.

Y Address Area Set

This instruction and parameter set up the Y address areas of the on-chip display data RAM.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
0	0	1	0	1	0	0	0	0	1	0	42
			Y start address set (Initial Status = 00H)								-
			Y end address set (Initial Status = 9FH)								-

The current Y address of the on-chip display data RAM is the Y start address by setting this instruction. In Y address count mode (X/Y = “H”), the Y address is increased from Y start address to Y end address. When Y address is equal to the Y end address, the X address is increased by 1 and the Y address returns to Y start address. The Y start and Y end addresses must be set as a pair and Y start address must be less than Y end address.

X Address Area Set

This instruction and parameter set up the X address areas of the on-chip display data RAM.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
0	0	1	0	1	0	0	0	0	1	1	43
			X start address set (Initial Status = 00H)								-
			X end address set (Initial Status = 7FH)								-

The current X address of the on-chip display data RAM is the X start address by setting this instruction. In X address count mode (X/Y = “L”), the X address is increased from X start address to X end address. When X address is equal to the X end address, the Y address is increased by 1 and the X address returns to X start address. The X start and X end address must be set as a pair and X start address must be less than X end address.

Bias Set

This instruction and parameter set up the Bias ratio of voltage booster.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
0	0	1	0	1	0	0	0	1	1	0	46
			0	BIAS2[2:0]			0	BIAS1[2:0]			-

BIAS1 : Voltage booster bias ratio in normal mode.
BIAS2 : Voltage booster bias ratio in partial mode.

BIAS2 : In partial mode			
BIAS2[2:0]			Voltage booster bias ratio
0	0	0	Operating under 1/5 bias
0	0	1	Operating under 1/6 bias
0	1	0	Operating under 1/7 bias
0	1	1	Operating under 1/8 bias
1	0	0	Operating under 1/9 bias
1	0	1	Operating under 1/10 bias
1	1	0	Operating under 1/11 bias
1	1	1	Operating under 1/12 bias

BIAS1 : In normal mode			
BIAS1[2:0]			Voltage booster bias ratio
0	0	0	Operating under 1/5 bias
0	0	1	Operating under 1/6 bias
0	1	0	Operating under 1/7 bias
0	1	1	Operating under 1/8 bias
1	0	0	Operating under 1/9 bias
1	0	1	Operating under 1/10 bias
1	1	0	Operating under 1/11 bias
1	1	1	Operating under 1/12 bias

Recommended maximum voltage of VCOMH – VCOML is 32V. When set up register that contrast control 3, contrast control 2, contrast control 1, Boosting Coefficient Set (BC1,BC2), Bias Set (BIAS1, BIAS2), be careful of VCOMH – VCOML is not over 32V.

Bias Level

The HDC1600 has 8 kinds of bias level (1/5 ~ 1/12 bias). VCOMH, VCOML, VSEGH, VSEGL voltage level is changed by Bias Set and Contrast Control and Boosting Coefficient Set instruction. Next figure is a LCD waveform by BIAS value.

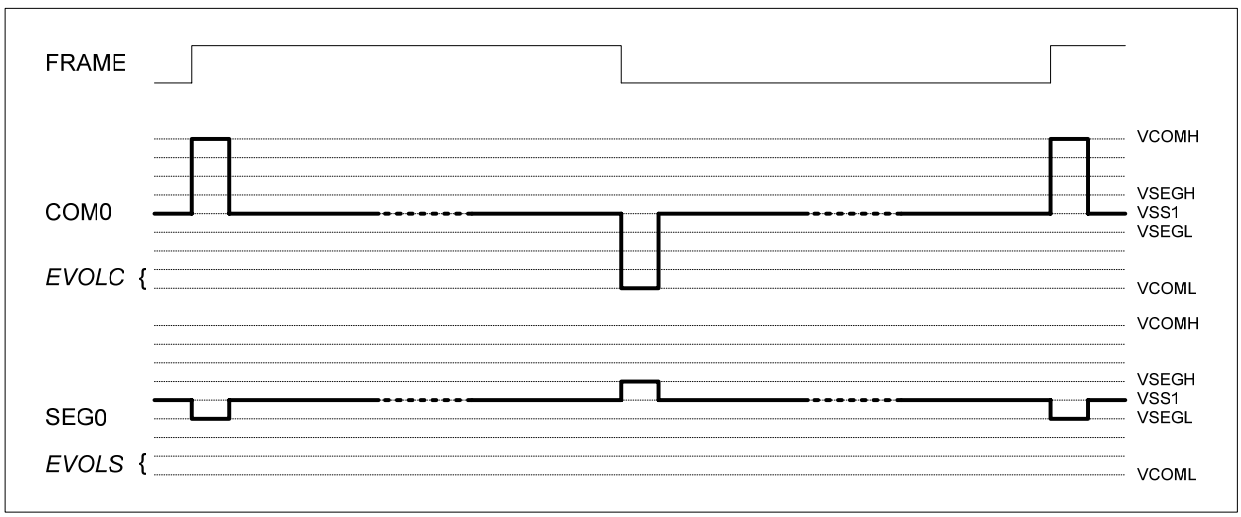


Figure 32. Voltage level of LCD Waveform by BIAS[2:0] = 3'b000 (1/5 bias)

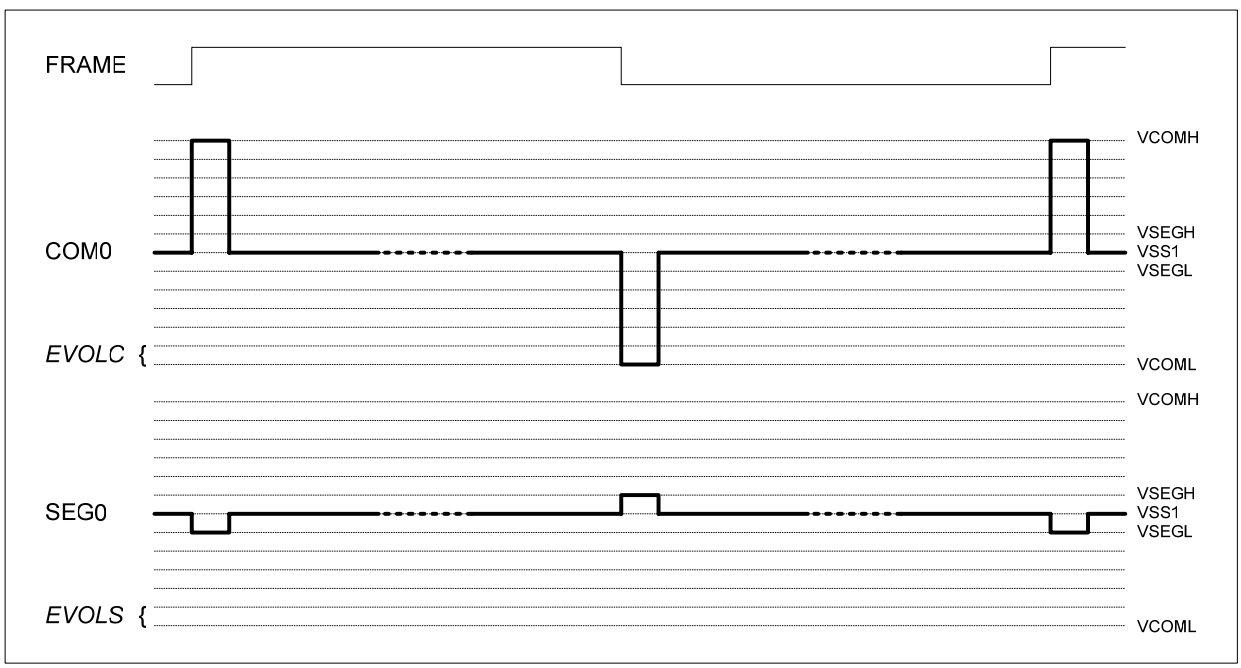


Figure 33. Voltage level of LCD Waveform by BIAS[2:0] = 3'b010 (1/7 bias)

Display ON/OFF

This instruction turn the display ON/OFF.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
0	0	1	0	1	0	1	0	0	0	DISP	50/51

DISP : Display ON/OFF control
- DISP = 0 : Display OFF (initial status).
- DISP = 1 : Display ON.

In case of being standby mode, Display ON does not work. This instruction is executed after standby mode off.

Function and Pin condition at Display OFF

Function / Pin	Condition
DC/DC booster(1'st, 2'nd, 3'rd)	ON (Operate)
SEG and COM outputs	VSS1

Function and Pin condition at Display ON

Function / Pin	Condition
DC/DC booster(1'st, 2'nd, 3'rd)	ON (Operate)
COM outputs	VCOMH or VSS1 or VCOML
SEG outputs	VSEGH or VSEGL

Specified Display Pattern Set

This instruction sets the specified display pattern.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
0	0	1	0	1	0	1	0	0	1	1	53
			0	0	0	0	0	0	SDP[1:0]		-

SDP : Specified display pattern set.
- SDP = 00 : Normal display.
- SDP = 01 : Reverse display : Display data reversing mode setting without the contents of the display RAM.
- SDP = 10 : Whole display pattern becomes OFF regardless of the RAM data.
- SDP = 11 : Whole display pattern becomes ON regardless of the RAM data.

Partial Display Mode Set

This instruction sets the partial display 1,2 mode enable/disable.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
0	0	1	0	1	0	1	0	1	0	1	55
			0	0	0	0	0	0	PD2EN	PD1EN	-

PD2EN : Partial display 2 mode enable/disable.
PD1EN : Partial display 1 mode enable/disable.

PD2EN	PD1EN	Display Mode
0	0	Normal display state (initial status)
0	1	Partial display 1 mode enable
1	0	Partial display 2 mode enable
1	1	Partial display 1 and Partial display 2 mode enable

Partial Display 1 Start Line Set

This instruction sets partial display 1 COMMON start line.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
0	0	1	0	1	0	1	0	1	1	0	56
			PDSL1[7:0]								-

When the partial display 1 mode is specified (PD1EN=1) to operate, partial display 1 start line for 1'st partial display picture is set by this register. Partial display 1 start line must be less than partial display 1 end line.

Partial Display 1 End Line Set

This instruction sets partial display 1 COMMON end line.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
0	0	1	0	1	0	1	0	1	1	1	57
			PDEL1[7:0]								-

When the partial display 1 mode is specified (PD1EN=1) to operate, partial display 1 end line for 1'st partial display picture is set by this register. Partial display 1 end line must be greater than partial display 1 start line.

Partial Display 1 Start Memory Set

This instruction sets partial display 1 Memory start line.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
0	0	1	0	1	0	1	1	0	1	0	5A
			PDSM1[7:0]								-

When partial display 1 mode is specified (PD1EN=1) to operate, partial display 1 start memory that corresponds partial display 1 start line for 1'st partial display picture is set by this register. Partial display 1 end memory is decided to the total line that adds the difference of partial display 1 start line and end line to the partial display 1 start memory.

MPE Mode ON/OFF

This instruction set up MPE mode.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
0	0	1	0	1	0	1	1	1	0	MPE	5C/5D

When MPE is ON, Moving picture control engine is in operation. so, Color-STN is react rapidly. Moving picture display image is looked naturally compare with MPE is OFF. When stopped image is displayed, MPE is to be OFF.

MPE : Moving picture enhancement mode ON/OFF.
- MPE = 0 : MPE mode OFF (initial status).
- MPE = 1 : MPE mode ON.

Partial Display 2 Start Line Set

This instruction sets partial display 2 COMMON start line.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
0	0	1	0	1	1	0	0	0	0	0	60
			PDSL2[7:0]								-

When the partial display 2 mode is specified (PD2EN=1) to operate, partial display 2 start line for 2'st partial display picture is set by this register. Partial display 2 start line must be less than partial display 2 end line.

Partial Display 2 End Line Set

This instruction sets partial display 2 COMMON end line.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
0	0	1	0	1	1	0	0	0	1	0	62
			PDEL2[7:0]								-

When the partial display 2 mode is specified (PD2EN=1) to operate, partial display 2 end line for 2'st partial display picture is set by this register. Partial display 2 end line must be greater than partial display 2 start line.

Partial Display 2 Start Memory Set

This instruction sets partial display 2 Memory start line.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
0	0	1	0	1	1	0	0	1	0	0	64
			PDSM2[7:0]								-

When partial display 2 mode is specified (PD2EN=1) to operate, partial display 2 start memory that corresponds partial display 2 start line for 2'nd partial display picture is set by this register. Partial display 1 end memory is decided to the total line that adds the difference of partial display 2 start line and end line to the partial display 2 start memory.

Relation between PDSL, PDEL, PDSM setting and COMMON / Display RAM

The COMMON port number corresponds to Y address of display RAM varies by COMDIR instruction, LCD duty, COMMON display start line register and display start line setting instruction.

When display start address was set to “0”.

The relation between COMMON port and line address of display RAM (MY) varies according to LCD duty and display start COMMON address setting register (PDSL). When COMDIR register is set to “0” COMMON line shift to upward direction, and when the value is “1”, COMON line shift to downward direction. When display start memory address (PDSM1, PDSM2) is set to “0”, the “MY” corresponds to memory starting position is “0”. The MY shift upward direction as display goes on.

When display start line was set except for “0”.

The relation between COMMON port and line address of display RAM, MY varies according to LCD duty and display start COMMON address setting register (PDSL). When COMDIR register is set to “0” COMMON line shift to upward direction, and when the value is “1”, COMMON line shift to downward direction. When display start memory address (PDSM1, PDSM2) is set to except for “0”, the “MY” corresponds to starting memory position is shifted by the amount of set value. The MY shifts upward direction as display goes on but when MY becomes over than 160, it changes to “0” and then upward shifts.

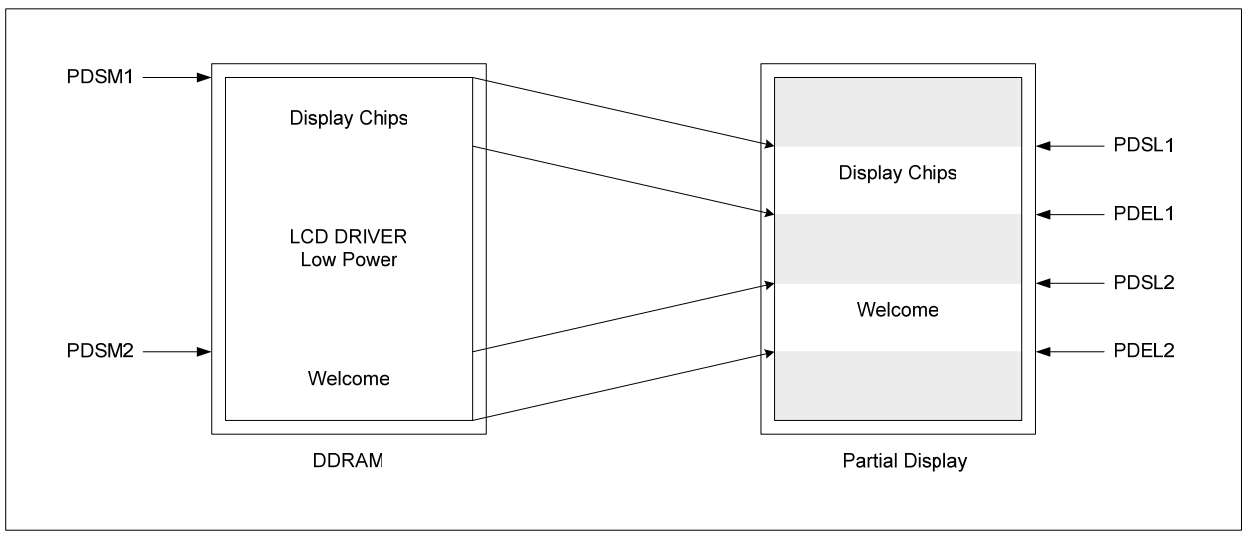
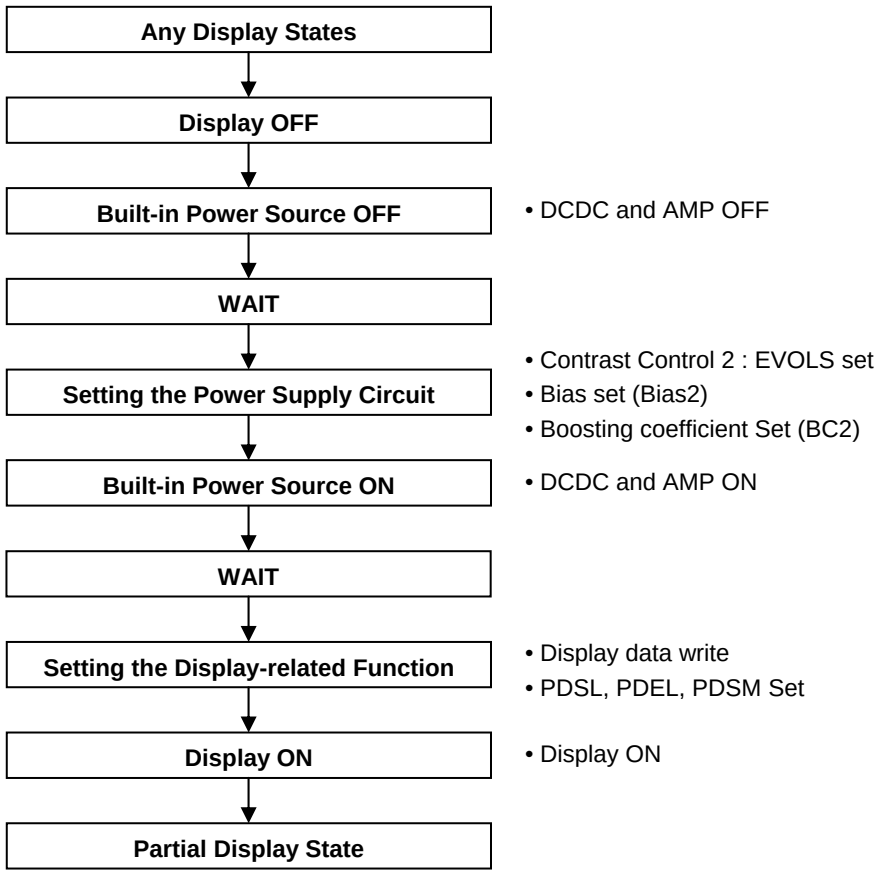


Figure 34. Partial Display Image Transfer

Partial Display Sequence



Common Scan Mode Set

This instruction turn the Common Scan Mode ON/OFF.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
0	0	1	0	1	1	0	0	1	1	CMS	66/67

This instruction is used to select the common scanning method. This IC can be placed in panel with less constraint at application.

CMS : Common scan mode ON/OFF.

- CMS = 0 : Scanning from start point to end point operates in sequence (initial status).
- CMS = 1 : Scanning from start point to end point operates in zigzag.

Next figure is a application diagram of COMSM value.

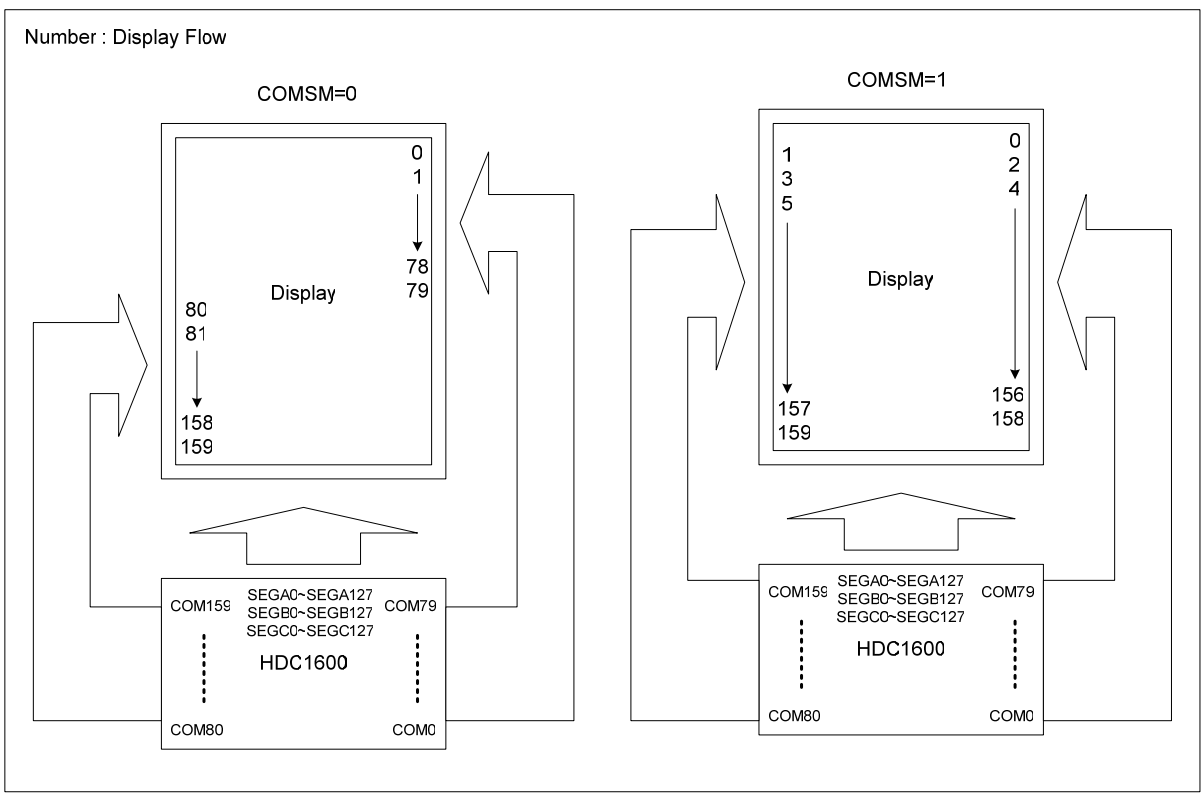


Figure 35. COMMON Display Flow of COMSM

Y address Decrement Set

This instruction sets Y address decrement.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
0	0	1	0	1	1	0	1	0	0	YDE	68/69

YDE : Y address decrement ON/OFF.

- YDE = 0 : Y address 00h => 9Fh (initial status).
- YDE = 1 : Y address 9Fh => 00h.

Next figure is DDRAM writing sequence with XDE.

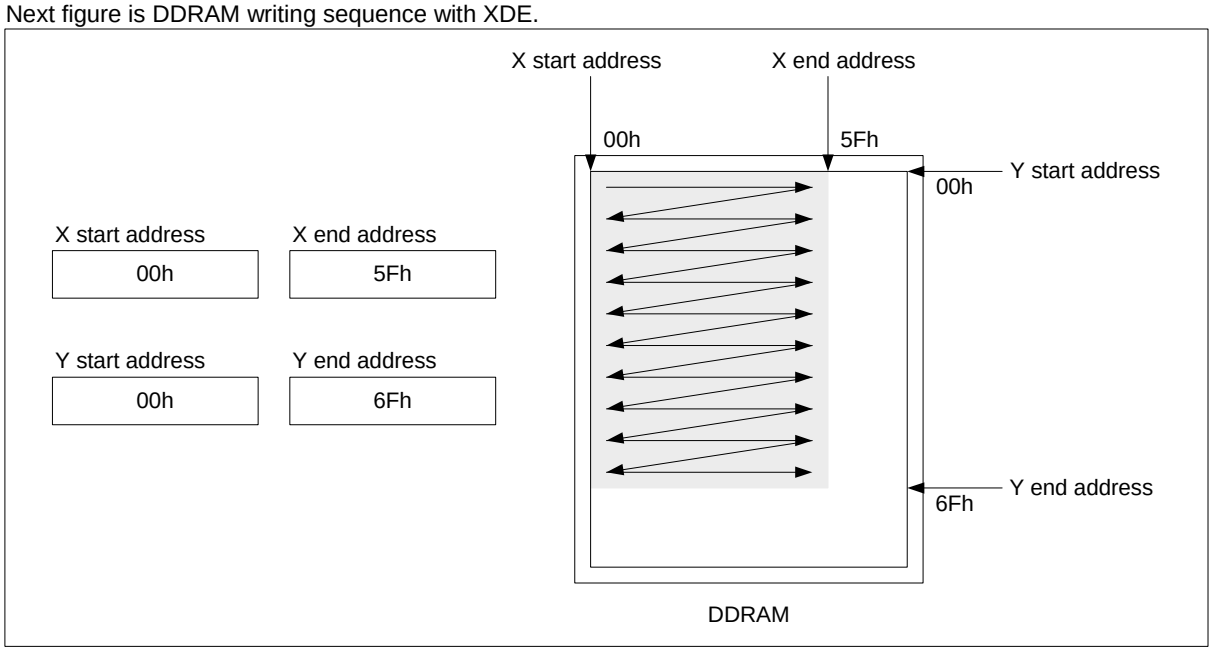


Figure 36. DDRAM Writing Sequence when YDE = L

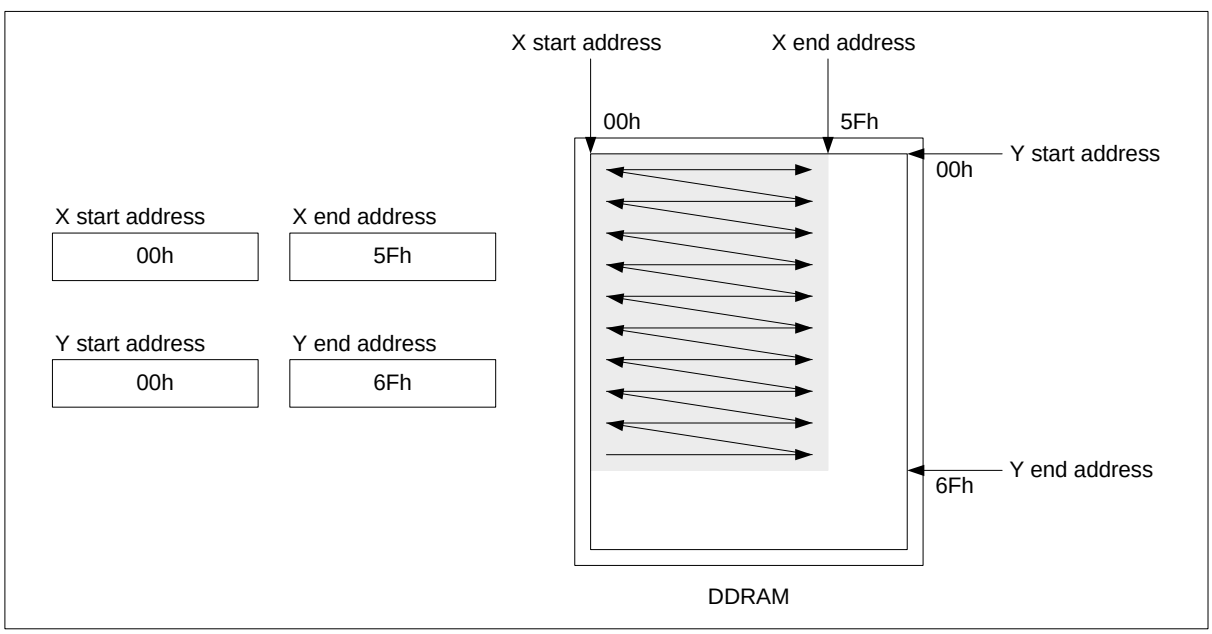


Figure 37. DDRAM Writing Sequence when YDE = H

Blank Time Set

This instruction sets blank time.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
0	0	1	0	1	1	0	1	0	1	0	6A
			BTEN	0	0	0	BTH[3:0]				-
			BTL[7:0]								-

When BTEN = 1, COMMON / SEGMENT is in VSS1 level during blank time.
BTEN : Blank timing ON/OFF.
- BTEN = 0 : Blank time is not exist (initial status).
- BTEN = 1 : Blank time is exist.

Blank time = (BT[11:0] + 1) * MCLK, (BT[11:0] = BTH[3:0],BTL[7:0], if BT[11:0] = 000h is forbidden.)

Next figure is a LCD waveform, when BTEN=1. Blank time is depend on BT[11:0] value.

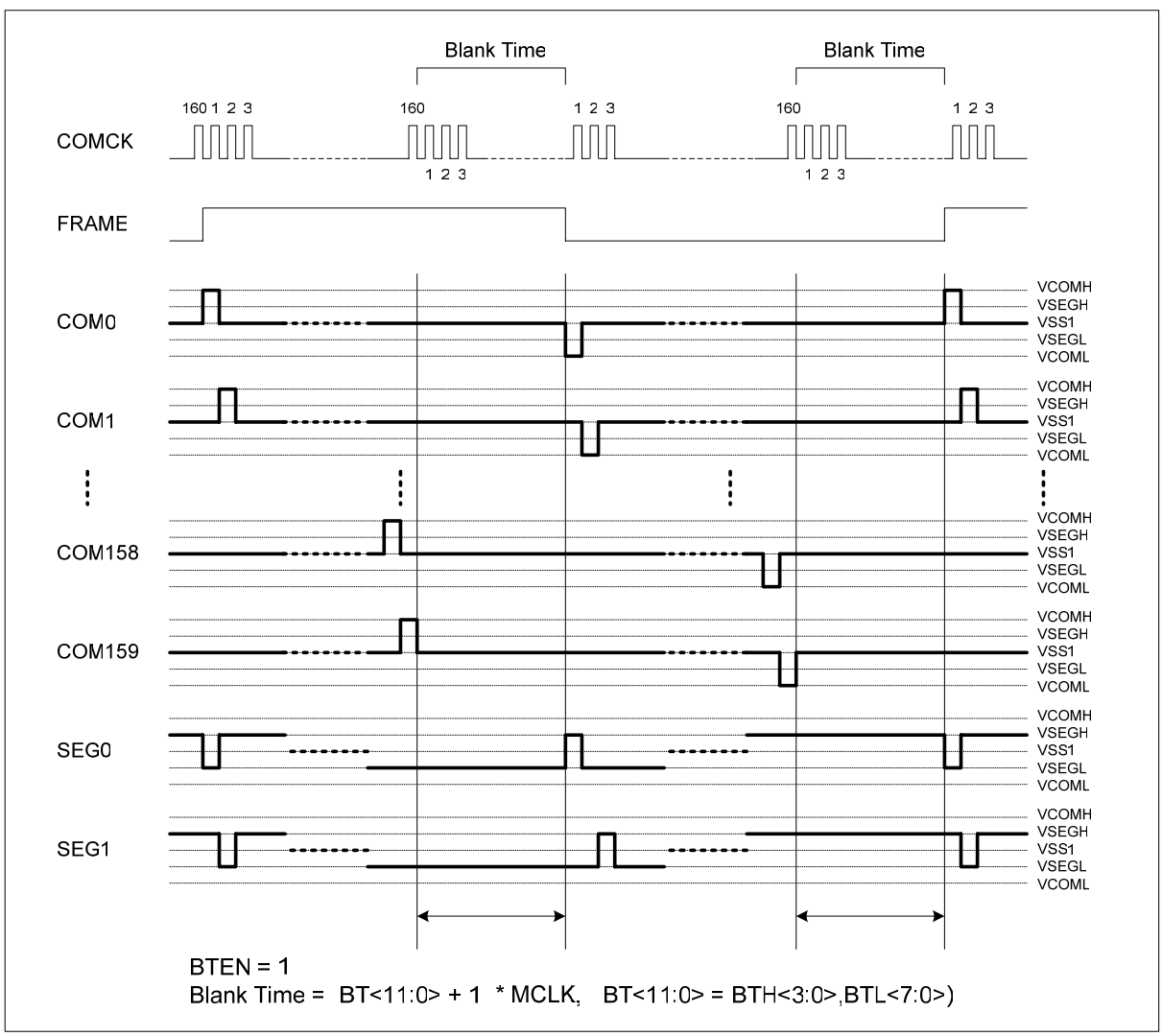


Figure 38. COMMON Display Flow of Blank Time

Gradation Red Palette Set

This instruction sets Gradation red palette data.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
0	0	1	0	1	1	1	0	0	0	0	70
			32 bytes of red palette data								-

To select the best suited red gradation level for LCD panel at variable gradation display mode, please set 32 red gradation register values among 128 gradation levels. The PWM in according to the selected gradation is driven through segment driver outputs, SEGA(0~127).

Gradation Green Palette Set

This instruction sets Gradation green palette data.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
0	0	1	0	1	1	1	0	0	0	1	71
			64 bytes of green palette data								-

To select the best suited green gradation level for LCD panel at variable gradation display mode, please set 64 green gradation register values among 128 gradation levels. The PWM in according to the selected gradation is driven through segment driver outputs, SEGB(0~127).

Gradation Blue Palette Set

This instruction sets Gradation blue palette data.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
0	0	1	0	1	1	1	0	0	1	0	72
			32 bytes of blue palette data								-

To select the best suited blue gradation level for LCD panel at variable gradation display mode, please set 32 blue gradation register values among 128 gradation levels. The PWM in according to the selected gradation is driven through segment driver outputs, SEGC(0~127).

Display Data Write

Display data write.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
1	0	1	Write Display Data								-

To write display data, RS is high status and 8bit Writing data is entered from DB[7:0].

Display Data Read

Display data read.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
1	1	0	Read Display Data								-

To read display data, RS is high status and 8bit Reading data is out from DB[7:0].

Status Read

This instruction indicates the internal status of the HDC1600.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
0	1	0	BSY	X/Y	0	PD2EN	PD1EN	STB	SDP0	DISP	-

DISP: (0 : Display OFF Status, 1 : Display ON Status)
SDP0: (Specified Display Pattern Set SDP[0])
STB: (0 : Standby Mode OFF Status, 1 : Standby Mode ON Status)
PD1EN: (0 : Partial Display Mode1 OFF, 1 : Partial Display Mode1 ON)
PD2EN: (0 : Partial Display Mode2 OFF, 1 : Partial Display Mode2 ON)
X/Y: (0 : X-address Count Mode, 1 : Y-address Count Mode)
BSY: (0 : No Busy, 1 : Busy)

User Trim Mode ON/OFF

This command is used to turn User trim mode ON/OFF.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
0	0	1	1	1	1	0	1	0	1	UTE	EA/EB

UTE : User trim mode ON/OFF.

- UTE = 0 : User trim mode OFF (initial status).
- UTE = 1 : User trim mode ON.

User Trim/Reg Selection

This command is used to select Trim value or user EVOL offset volume register value.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
0	0	1	1	1	1	0	1	1	0	0	EC
			0	0	0	0	0	0	0	UTS	-

UTS : User trim value or register value selection.

- UTS = 0 : User trim value selection (initial status).
- UTS = 1 : User EVOL offset volume register value selection.

User EVOL Offset Volume Set

This command is used to set offset value x (+31 to -31) to electronic volume (1 step=3mV).

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
0	0	1	1	1	1	0	1	1	0	1	ED
			0	0	UTOV[5:0]						-

UTOV[5:0] : User trim value.

UTOV[5:0]						User Trim EVOL Offset
0	1	1	1	1	1	+31
0	1	1	1	1	0	+30
⋮						⋮
0	0	0	0	0	1	+1
0(1)	0	0	0	0	0	0
1	0	0	0	0	1	-1
⋮						⋮
1	1	1	1	1	0	-30
1	1	1	1	1	1	-31

User Trim Write Enable/Disable

This command is used to write offset value (UTOV[5:0]) into user trim cells.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
0	0	1	1	1	1	0	1	1	1	UWT	EE/EF

UWT : User trim write enable/disable.

- UWT = 0 : User trim write disable (initial status).
- UWT = 1 : User trim write enable.

Test Mode1

This Instruction is for testing IC. User is not permitted to access. if access, have to reset.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
0	0	1	0	1	0	1	1	1	1	0	5E

Test Mode2

This Instruction is for testing IC. User is not permitted to access. if access, have to reset.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
0	0	1	0	1	1	0	1	0	1	1	6D

Test Mode3

This Instruction is for testing IC. User is not permitted to access. if access, have to reset.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
0	0	1	0	1	1	0	1	1	1	1	6F

Test Mode4

This Instruction is for testing IC. User is not permitted to access. if access, have to reset.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
0	0	1	1	0	0	0	0	0	0	0	80

Test Mode5

This Instruction is for testing IC. User is not permitted to access. if access, have to reset.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
0	0	1	1	0	0	0	0	0	0	1	81

Test Mode6

This Instruction is for testing IC. User is not permitted to access. if access, have to reset.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
0	0	1	1	1	1	1	1	0	0	0	F8

Test Mode7

This Instruction is for testing IC. User is not permitted to access. if access, have to reset.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
0	0	1	1	1	1	1	1	0	0	1	F9

Test Mode8

This Instruction is for testing IC. User is not permitted to access. if access, have to reset.

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.
0	0	1	1	1	1	1	1	0	1	0	FA

11. INSTRUCTION and PARAMETER

Instruction Name	Hex.	Para.	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Oscillation Mode Set	02	1	0	0	0	0	0	0	1	0
			0	0	0	0	EXTD	OSCDE	EXTM	OSCME
Driver Output Mode Set	10	1	0	0	0	1	0	0	0	0
			0	0	DLN[1:0]		0	SDIR	SWP	0
Boosting Coefficient Set	22	1	0	0	1	0	0	0	1	0
			0	BC2[2:0]			0	BC1[2:0]		
DCDC Clock Frequency Set	24	1	0	0	1	0	0	1	0	0
			0	DCK2[2:0]			0	DCK1[2:0]		
DCDC and AMP ON/OFF Set	26	1	0	0	1	0	0	1	1	0
			EXDC	0	0	0	AMPON	DCDC3	DCDC2	DCDC1
Temperature Compensation Set	28	1	0	0	1	0	1	0	0	0
			0	0	0	0	0	TCS[2:0]		
Contrast Control(3) : EVOLC	29	1	0	0	1	0	1	0	0	1
			0	0	Contrast3[5:0]					
Contrast Control(1) : EVOLS 1	2A	1	0	0	1	0	1	0	1	0
			Contrast1[7:0]							
Contrast Control(2) : EVOLS 2	2B	1	0	0	1	0	1	0	1	1
			Contrast2[7:0]							
Standby Mode ON/OFF	2C/2D	-	0	0	1	0	1	1	0	STB
DDRAM Burst Mode ON/OFF	2E/2F	-	0	0	1	0	1	1	1	BST
N-Line Inversion Set	34	1	0	0	1	1	0	1	0	0
			NLION	NLI[6:0]						
Main Clock Frequency Set	36	1	0	0	1	1	0	1	1	0
			MDIV[1:0]		MCLK[5:0]					
Entry Mode Set	40	1	0	1	0	0	0	0	0	0
			0	0	0	0	HL	MDI	X/Y	RMW
Y-address Area Set	42	2	0	1	0	0	0	0	1	0
			Y start address set							
			Y end address set							
X-address Area Set	43	2	0	1	0	0	0	0	1	1
			X start address set							
			X end address set							
Bias Set	46	1	0	1	0	0	0	1	1	0
			0	BIAS2[2:0]			0	BIAS1[2:0]		
Display ON/OFF	50/51	-	0	1	0	1	0	0	0	DISP
Specified Display Pattern Set	53	1	0	1	0	1	0	0	1	1
			0	0	0	0	0	0	SDP[1:0]	
Partial Display Mode Set	55	1	0	1	0	1	0	1	0	1
			0	0	0	0	0	0	PD2EN	PD1EN
Partial Display 1 Start Line Set	56	1	0	1	0	1	0	1	1	0
			PDSL1[7:0]							
Partial Display 1 End Line Set	57	1	0	1	0	1	0	1	1	1
			PDEL1[7:0]							
Partial Display 1 Start Memory Set	5A	1	0	1	0	1	1	0	1	0
			PDSM1[7:0]							
MPE Mode ON/OFF	5C/5D	-	0	1	0	1	1	1	0	MPE
Partial Display 2 Start Line Set	60	1	0	1	1	0	0	0	0	0
			PDSL2[7:0]							
Partial Display 2 End Line Set	62	1	0	1	1	0	0	0	1	0
			PDEL2[7:0]							
Partial Display 2 Start Memory Set	64	1	0	1	1	0	0	1	0	0
			PDSM2[7:0]							

(Continued)

Instruction Name	Hex.	Para.	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Common Scan Mode Set	66/67	-	0	1	1	0	0	1	1	CMS
Y-address Decrement Set	68/69	-	0	1	1	0	1	0	0	YDE
Blank Time Set	6A	2	0	1	1	0	1	0	1	0
			BTEN	0	0	0	BTH[3:0]			
			BTL[7:0]							
Gradation Red Palette Set	70	32	0	1	1	1	0	0	0	0
			32 bytes of red palette data							
Gradation Green Palette Set	71	64	0	1	1	1	0	0	0	1
			64 bytes of green palette data							
Gradation Blue Palette Set	72	32	0	1	1	1	0	0	1	0
			32 bytes of blue palette data							
User Trim Mode ON/OFF	EA/EB	-	1	1	1	0	1	0	1	UTE
User Trim/Reg Selection	EC	1	1	1	1	0	1	1	0	0
			0	0	0	0	0	0	0	UTS
User EVOL Offset Volume Set	ED	1	1	1	1	0	1	1	0	1
			0	0	UTOV[5:0]					
User Trim Write Enable/Disable	EE/EF	-	1	1	1	0	1	1	1	UWT

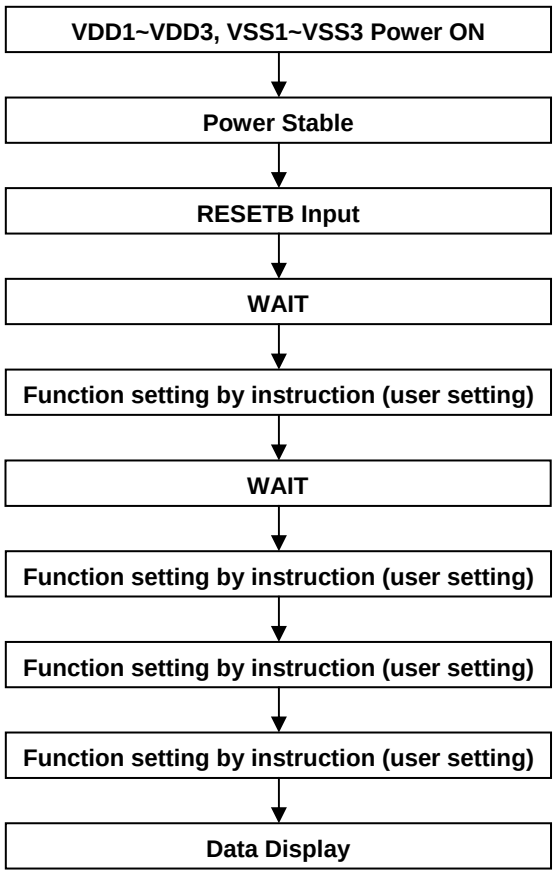
12. RESET OPERATION

When RESETB becomes “L”, following procedure is occurred.

- Oscillation Mode Set
  - *EXTD = 0 (Internal DCDC clock input)*
  - *OSCDE = 0 (Internal DCDC oscillator disable)*
  - *EXTM = 0 (Internal Main oscillator input)*
  - *OSCME = 0 (Internal Main oscillator disable)*
- Driver Output Mode Set
  - *DLN[1:0] = 10b (Display Duty : 1/160)*
  - *SDIR = 0 (Writing display data from X address 00h to 7Fh)*
  - *SWP = 0 (normal state)*
- Boosting Coefficient Set
  - *BC1 = 00 (2-Times Boosting)*
  - *BC2 = 00 (2-Times Boosting)*
- DCDC Clock Frequency Set
  - *DIV1 = 000b: 4.0 kHz*
  - *DIV2 = 000b: 4.0 kHz*
- *DC/DC and AMP ON/OFF Set*
  - *EXDC = 0 (Internal DCDC Power Circuit.*
  - *AMPON = 0 (Built-in VSEGH Op-amp. OFF)*
  - *DCDC1 = 0 (Built-in 1’st booster OFF)*
  - *DCDC2 = 0 (Built-in 2’nd booster OFF)*
  - *DCDC3 = 0 (Built-in 3’rd booster OFF)*
- *Temperature Compensation Set*
  - *TCS[2:0] = 000 (0.0%/degC)*
- *Contrast Control*
  - *EVOLS, EVOLC = 00h (1.035V)*
- *Standby Mode ON*
- *DDRAM Burst Mode OFF*
- *N-line inversion*
  - *NLION = 0 (N-line inversion OFF)*
- *Main Clock Frequency Set*
  - *MDIV[1:0] = 00b (No division)*
  - *MCLK[5:0] = 000000b (2.00MHz)*
- *Entry Mode Set*
  - *HL = 0 (1’st 8bit-data : MSB, 2’nd 8bit-data : LSB)*
  - *MDI = 0 (Memory Data Inversion OFF)*
  - *X/Y = 0 (X-address Count Mode)*
  - *RMW = 0 (Read modify write mode OFF)*
- *Y start address: 0, Y end address: 159*
- *X start address: 0, X end address: 127*
- *Bias Set*
  - *Bias1[2:0] = 000b: 1/5 bias*
  - *Bias2[2:0] = 000b: 1/5 bias*
- *Display OFF*
- *Specified Display Pattern Set*
  - *SDP[1:0] = 00 (Normal display)*
- *Partial Display 1 Mode : OFF, Partial Display 2 Mode : OFF*
- Common Scan Mode OFF
- Y address Decrement OFF
- Blank Time Disable
- Red/Green/Blue Gradation Palette : Initial Value

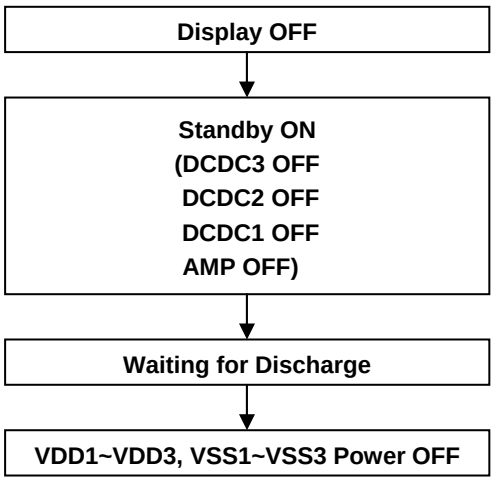
13. POWER ON/OFF SEQUENCE

Power ON Sequence



notice) If the voltage level of VDD3 and VDD1 are different , VDD1 should be inputted first.

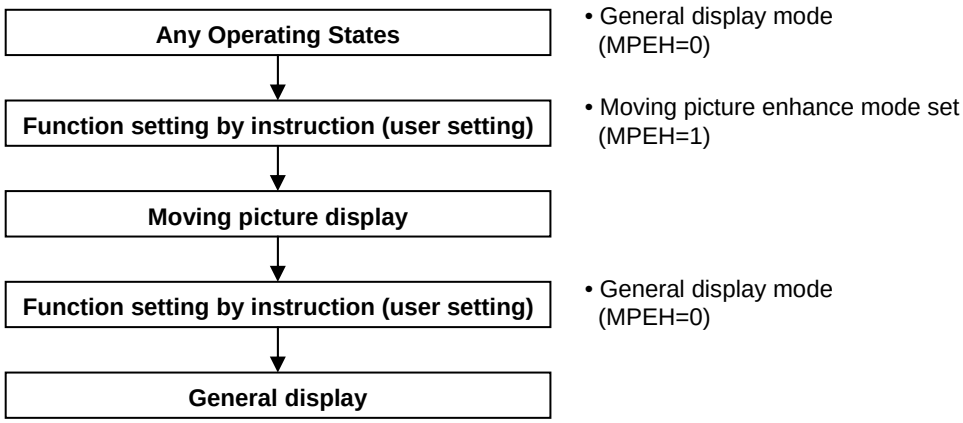
Power OFF Sequence



notice) Before turning off the power, be sure to execute STBY instruction to make LCD driver output OFF state. And if the level of VDD3 and VDD1 are different (not common but different source), VDD3 terminal should be turned OFF during VDD1 terminal voltage maintain voltage level.

14. MPE ON/OFF SEQUENCE

It improves the response time of any LCD panel as much as 30~40% of normal speed, so it could make the CSTN panel used for playing moving pictures as TFT panel.



15. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Condition	Rating	Unit
Supply Voltage Range	VDD1	VSS1 = VSS2 = VSS3 = 0V Ta=25℃	-0.3 ~ +3.6	V
	VDD2		-0.3 ~ +3.6	V
	VDD3		-0.3 ~ +3.6	V
LCD Supply Voltage Range	VCOMH		-0.3 ~ +18.0	V
	VCOML		+0.3 ~ -18.0	V
	VSEGH		-0.3 ~ +1.8	V
	VSEGL		+0.3 ~ -1.8	V
Input Voltage Range	$V_{IN(*1)}$		-0.3 ~ +3.6	V
Storage Temperature Range	T_{STG}		-45 ~ +125	℃

(*1) DB15~DB0, RESETB, CS1B, CS2, PS, RS, WRB, RDB, MPU[1:0], CDIR, EXMCLK, EXDCCLK, EXVREF, TEST Pin.

RECOMMENDED OPERATING CONDITIONS

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	VDD1	1.8	-	3.3	V
	VDD2	2.4	-	3.3	V
	$VDD3_{(*1)}$	2.4	-	3.3	V
Operation Temperature	T_{OPR}	-30	-	+70	℃

(*1) When the boosting circuit is used, supply voltage VDD3 should be used within the limit.
When driving LCD panel by use of internal boosting circuit, it is possible to short VDD2 and VDD3.

DC CHARACTERISTICS 1

(VDD1=1.8~3.3V, VDD2=VDD3=2.4~3.3V, VSS1=VSS2=VSS3=0.0V, Ta=-30~+70℃)

Item		Symbol	Condition	Min	Typ	Max	Unit	Remarks
Input Voltage	High	V_{IH}	-	0.8VDD1	-	VDD1	V	(*1)
	Low	V_{IL}	-	0	-	0.2VDD1	V	(*1)
Output Voltage	High	V_{OH}	I_{OH} = -0.5㎃	VDD1-0.4	-	-	V	(*2)
	Low	V_{OL}	I_{OL} = 0.5㎃	0	-	0.4	V	(*2)
Input Leakage Current		I_{IL}	VI = VSS1 or VDD1	-1.0	-	1.0	㎂	(*1)
Output Leakage Current		I_{OL}	VI = VSS1 or VDD1	-3.0	-	3.0	㎂	(*2)
Main Oscillator Frequency Tolerance		F_{MOSC}	VDD2 = 3.0V MCLK[7:0] = 00h	1.90	2.00	2.10	㎒	-
DCDC Oscillator Frequency Tolerance		F_{DOSC}	VDD2 = 3.0V DCK1[2:0] = 110b	24.0	32.0	40.0	㎑	-
LCD Driving Voltage Input Range(*3)		V_{COMH}	External Power Supply Mode	5.0	-	16.0	V	VCOMH
		V_{COML}		-16.0	-	-5.0	V	VCOML
		V_{SEGH}		1.0	-	1.8	V	VSEGH
		V_{SEGL}		-1.8	-	-1.0	V	VSEGL
Voltage Reference Input Range(*4)		V_{EXR}	TCS[2:0] = 111b	0.9	-	2.0	V	EXVREF
Regulator Output Range		V_{REG}	-	1.95	-	2.30	V	PWREG
LCD Driver Output ON Resistance	SEG	R_{ONSEG}	VSEGH = 1.5V, VSEGL = -1.5V, Ta = 25℃, I_{LOAD}=50㎂	-	5.0	7.5	㏀	SEG_n (n = 0~127)
	COM	R_{ONCOM}	VCOMH = 9.0V, VCOML = -9.0V, Ta = 25℃, I_{LOAD}=100㎂	-	500	750	Ω	COM_n (n = 0~159)
Current Consumption		I_{STB}	Standby ON	-	1.5	10.0	㎂	(*5)
		I_{DD}	VDD1=VDD2 =VDD3=3.0V, DCDC1,2,3, AMP=ON, External Cap. = 1.0㎌, EVOLC=EVOLS=1.4V BIAS1 = 1/12, BC1 = 6X, Ta = 25℃, Display Line =160, F_{MOSC} = 2.0 ㎒, F_{DOSC} = 4.0 ㎑, No Load, No access, All White Pattern	-	TBD	TBD	㎂	-

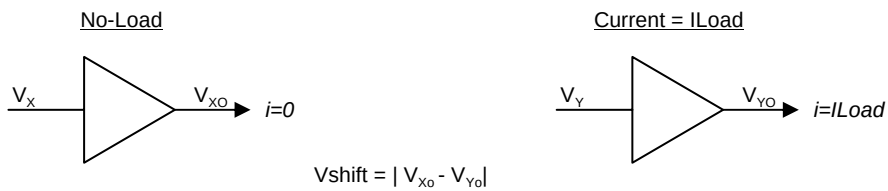
(*1) DB15~DB0, RESETB, CS1B, CS2, PS, RS, WRB, RDB, MPU[1:0], CDIR, EXMCLK, EXDCCLK Pins.
(*2) DB15~DB0 Pins.
(*3) Please keep the relation, VCOMH > VSEGH > VSS1 > VSEGL > VCOML, when the internal boosting circuit is not used.
(*4) When the internal reference voltage circuit is not used, reference voltage VREF should be used within the limit.
(*5) VDD1, VDD2, VDD3 Pins current, when source clock is stopped, chip selection (CS1B=VDD1) is non-selection status and no load.

DC CHARACTERISTICS 2

(VDD1=1.8~3.3V, VDD2=VDD3=2.4~3.3V, VSS1=VSS2=VSS3=0.0V, Ta=-30~+70℃)

Item	Symbol	Condition	Min	Typ	Max	Unit	Remarks
Voltage Shift Range(*1)	ΔV_{COMH}	I_{SOURCE} = 80μA	-	-	200	mV	VCOMH
	ΔV_{SEGH}	I_{SOURCE} = 250μA	-	-	50	mV	VSEGH
	ΔV_{SEGL}	I_{SINK} = 250μA	-	-	50	mV	VSEGL
	ΔV_{COML}	I_{SINK} = 80μA	-	-	200	mV	VCOML

(*1) Voltage shift means output voltage deference between output current = Iload and no-load.
Refer to the following figure. (in case of source current mode)



DC CHARACTERISTICS 3

(VDD1=1.8~3.3V, VDD2=VDD3=2.4~3.3V, VSS1=VSS2=VSS3=0.0V, Ta=-30~+70℃)

Item	Symbol	Condition	Min	Typ	Max	Unit	Remarks
Tolerance of Bias Ratio	ΔV_{CH} $\Delta V_{CL(*1)}$	No load	-500	-	500	mV	VCOMH VCOML
Temperature Compensation	ΔV_T	-	-0.02	-	0.02	%/℃	VSEGH
Tolerance of Contrast Step of VSEGH	ΔV_{STEP}	-	2.0	3.0	4.0	mV	VSEGH
VSEGH Voltage Range	ΔV_{SHR}	Contrast Set = FFh	1.75	1.80	1.85	V	VSEGH
		Contrast Set = 00h	0.985	1.035	1.085	V	VSEGH
Voltage Booster Offset Voltage(*2)	ΔV_{CHL}	I_{LOAD} = -100μA(VCOMH) I_{LOAD} = 100μA(VCOML)	-	-	150	mV	Fig.1
	ΔV_{SHL}	I_{LOAD} = -100μA(VSEGH) I_{LOAD} = 100μA(VSEGL)	-	-	70	mV	Fig.2

(*1) Tolerance of bias ratio definition
ΔVCH = (VCOMH - VSS1) - VSEGH / (Bias-1)
ΔVCL = (VSS1 - VCOML) - VSEGH / (Bias-1)
(*2) Voltage Range
VCOMH=5.0~16.0V, VCOML=-5.0~-16.0V, VSEGH=1.0~1.8V, VSEGL=-1.0~-1.8V

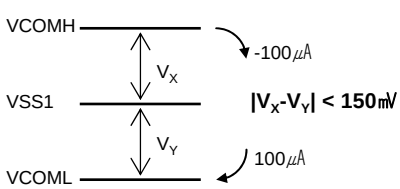


Fig.1 Offset voltage definition (VCOMH,VCOML)

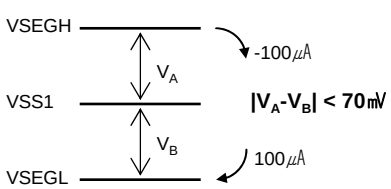
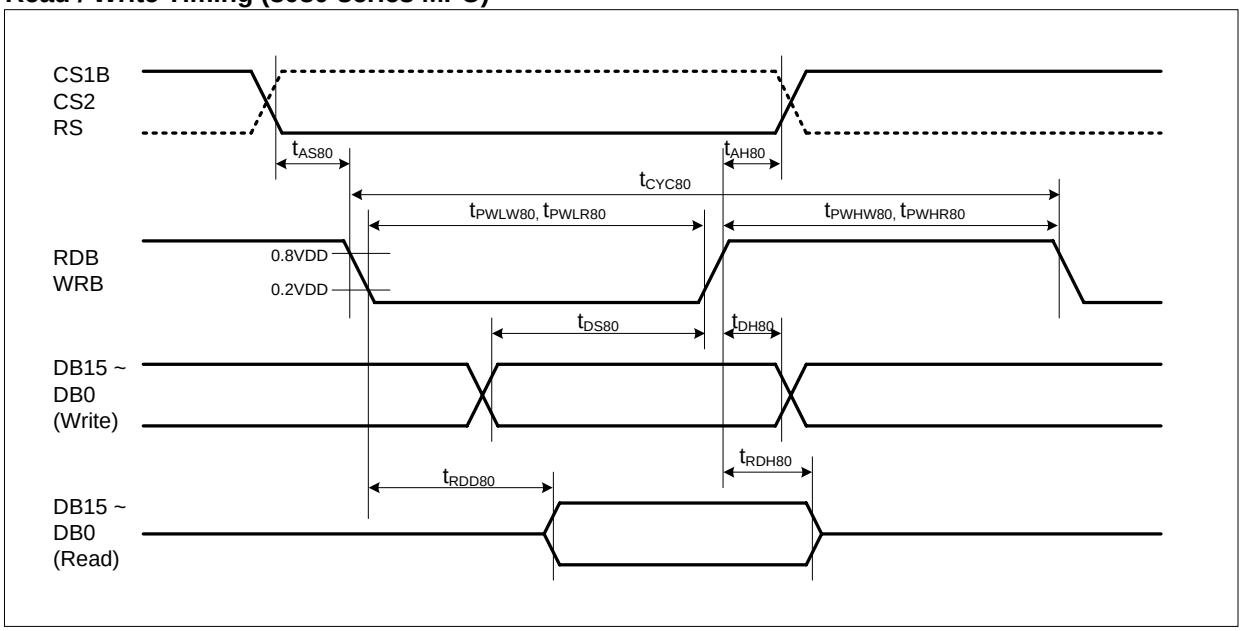


Fig.2 Offset voltage definition (VSEGH,VSEGL)

AC CHARACTERISTICS

Read / Write Timing (8080-series MPU)



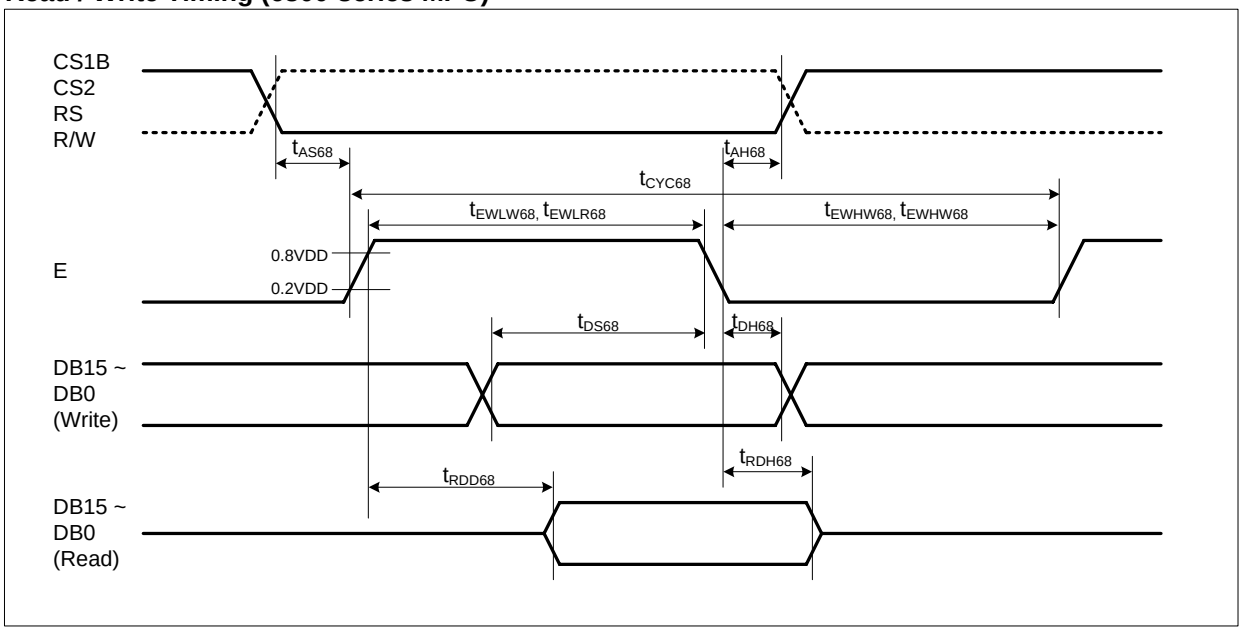
* tPWLW80 and tPWLR80 is specified in the overlapped period when CS1B is low (CS2 is high) and WRB(RDB) is low.

Table 11. AC Characteristics (8080-series Parallel Mode)

(VDD1=1.8~3.3V, VSS1=0.0V, Ta=-30~+70℃)

Item	Signal	Symbol	Condition	Min		Max		Unit
				3.3V	1.8V	3.3V	1.8V	
Address setup time	RS	t_{AS80}	-	0	0	-	-	ns
Address hold time	CS1B	t_{AH80}	-	0	0	-	-	ns
System cycle time	WRB	t_{CYC80}	-	100	250	-	-	ns
Write “L” pulse width	WRB	t_{PWLW80}	-	35	80	-	-	ns
Write “H” pulse width	WRB	t_{PWHW80}	-	35	80	-	-	ns
Read “L” pulse width	RDB	t_{PWHR80}	-	35	80	-	-	ns
Read “H” pulse width	RDB	t_{PWLR80}	-	35	80	-	-	ns
Data setup time	DB[15:0]	t_{DS80}	-	30	70	-	-	ns
Data hold time	DB[15:0]	t_{DH80}	-	5	10	-	-	ns
Read data output time	DB[15:0]	t_{RDD80}	CL=15pF	60	110	-	-	ns
Output data hold time	DB[15:0]	t_{RDH80}	-	10	15	-	-	ns

Read / Write Timing (6800-series MPU)



* tPWLW68 and tPWLR68 is specified in the overlapped period when CS1B is low (CS2 is high) and WRB(RDB) is low.

Table 12. AC Characteristics (6800-series Parallel Mode)

(VDD1=1.8~3.3V, VSS1=0.0V, Ta=-30~+70℃)

Item	Signal	Symbol	Condition	Min		Max		Unit
				3.3V	1.8V	3.3V	1.8V	
Address setup time	RS	t_{AS68}	-	0	0	-	-	ns
Address hold time	CS1B	t_{AH68}	-	0	0	-	-	ns
System cycle time	RDB(E)	t_{CYC68}	-	100	250	-	-	ns
Write “L” pulse width	RDB(E)	t_{PWLW68}	-	35	80	-	-	ns
Write “H” pulse width	RDB(E)	t_{PWHW68}	-	35	80	-	-	ns
Read “L” pulse width	RDB(E)	t_{PWHR68}	-	35	80	-	-	ns
Read “H” pulse width	RDB(E)	t_{PWLR68}	-	35	80	-	-	ns
Data setup time	DB[15:0]	t_{DS68}	-	30	70	-	-	ns
Data hold time	DB[15:0]	t_{DH68}	-	5	10	-	-	ns
Read data output time	DB[15:0]	t_{RDD68}	CL=15pF	60	110	-	-	ns
Output data hold time	DB[15:0]	t_{RDH68}	-	10	15	-	-	ns

Serial Data Interface Timing

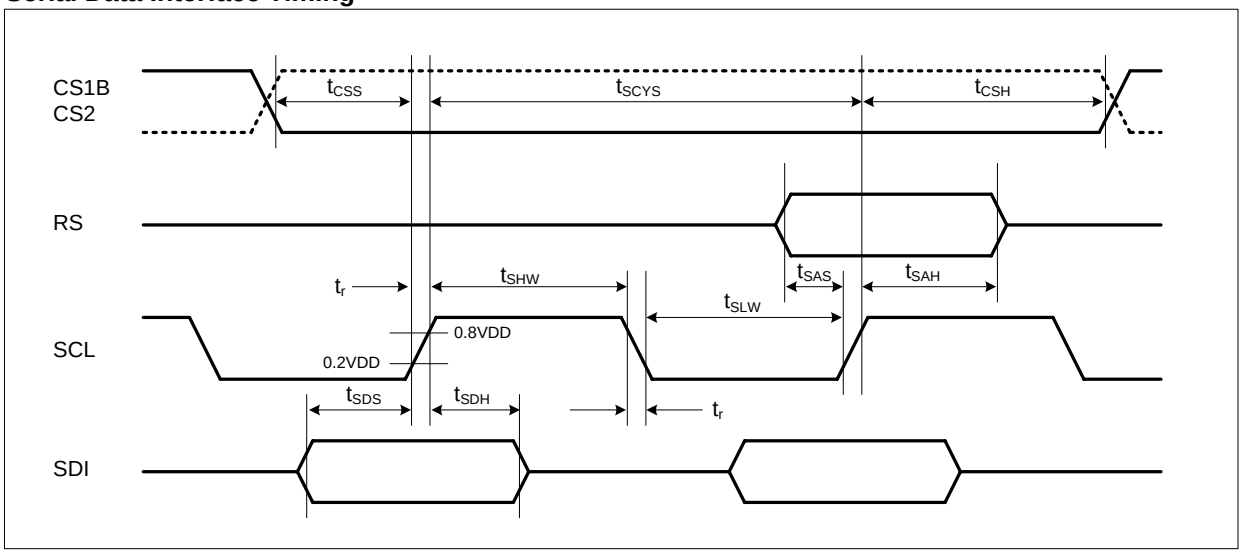


Table 13. Serial Data Interface Timing

(VDD1=1.8~3.3V, VSS1=0.0V, Ta=-30~+70℃)

Item	Signal	Symbol	Condition	Min		Max		Unit
				3.3V	1.8V	3.3V	1.8V	
SCL Cycle Time	SCL	t_{CSC}	-	60	120	-	-	ns
SCL High Pulse Width	SCL	t_{SHW}	-	20	40	-	-	ns
SCL Low Pulse Width	SCL	t_{SLW}	-	20	40	-	-	ns
SDI Setup Time	SDI	t_{SDS}	-	20	40	-	-	ns
SDI Hold Time	SDI	t_{SDH}	-	20	40	-	-	ns
RS Setup Time	RS	t_{SAS}	-	20	40	-	-	ns
RS Hold Time	RS	t_{SAH}	-	20	40	-	-	ns
Chip Select Setup Time	CS1B	t_{CSS}	-	20	40	-	-	ns
Chip Select Hold Time	CS1B	t_{CSH}	-	20	40	-	-	ns

Reset Input Timing

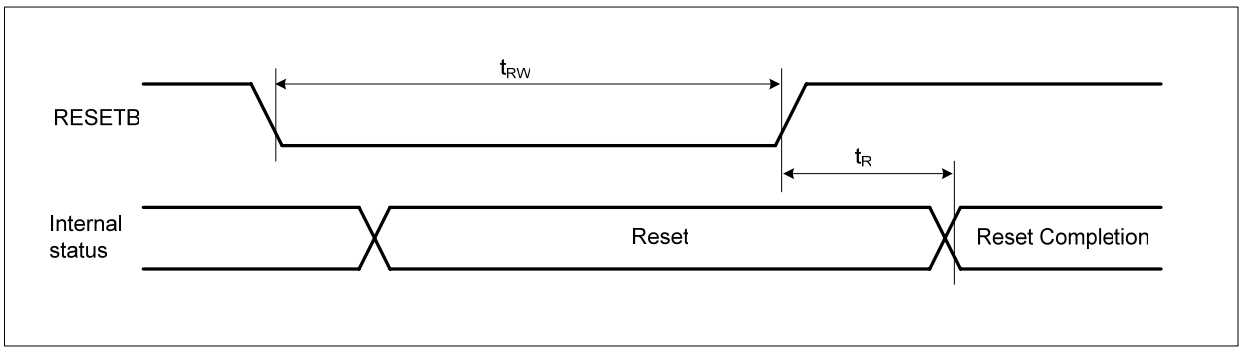


Table 14. AC Characteristics (Reset Mode)

(VDD1=1.8~3.3V, VSS1=0.0V, Ta=-30~+70℃)

Item	Signal	Symbol	Condition	Min		Max		Unit
				3.3V	1.8V	3.3V	1.8V	
Reset Low Pulse Width	RESETB	t_{RW}	-	10	10	-	-	μs
Reset Time	RESETB	t_R	-	1	1.5	-	-	μs

16. SYSTEM APPLICATION DIAGRAM

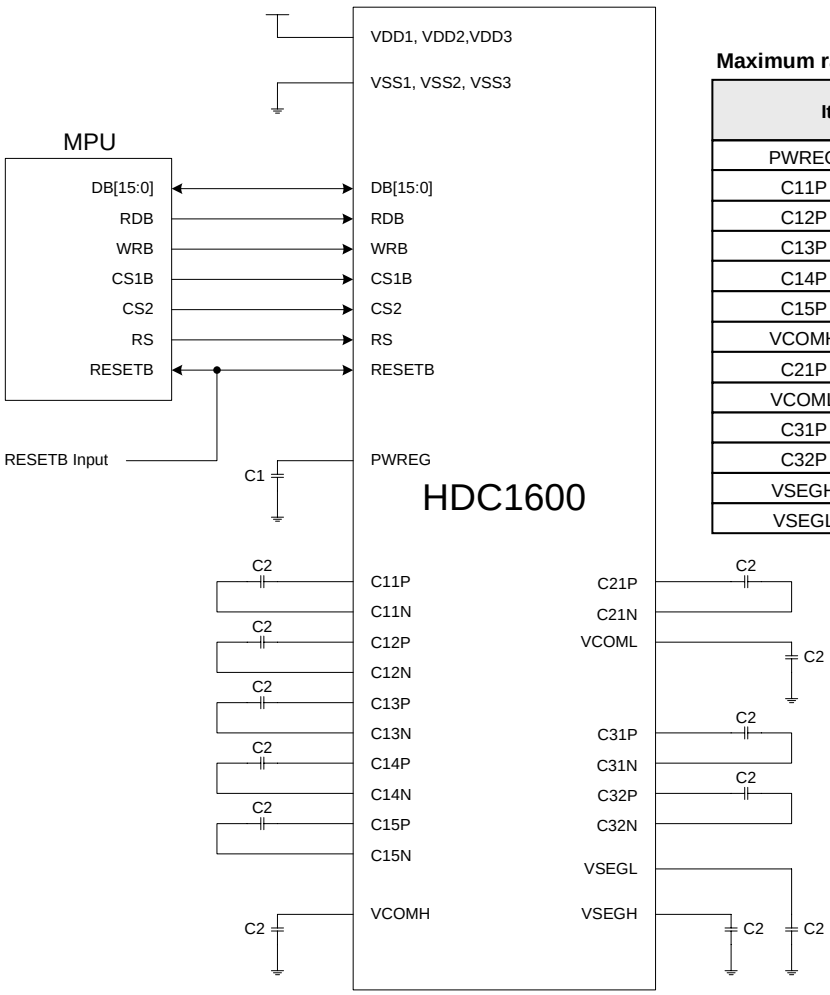
Internal Power Mode

Values of external components

Item	Capacitance
C1	1.0 ~ 4.7㎌
C2	1.0 ~ 2.2㎌

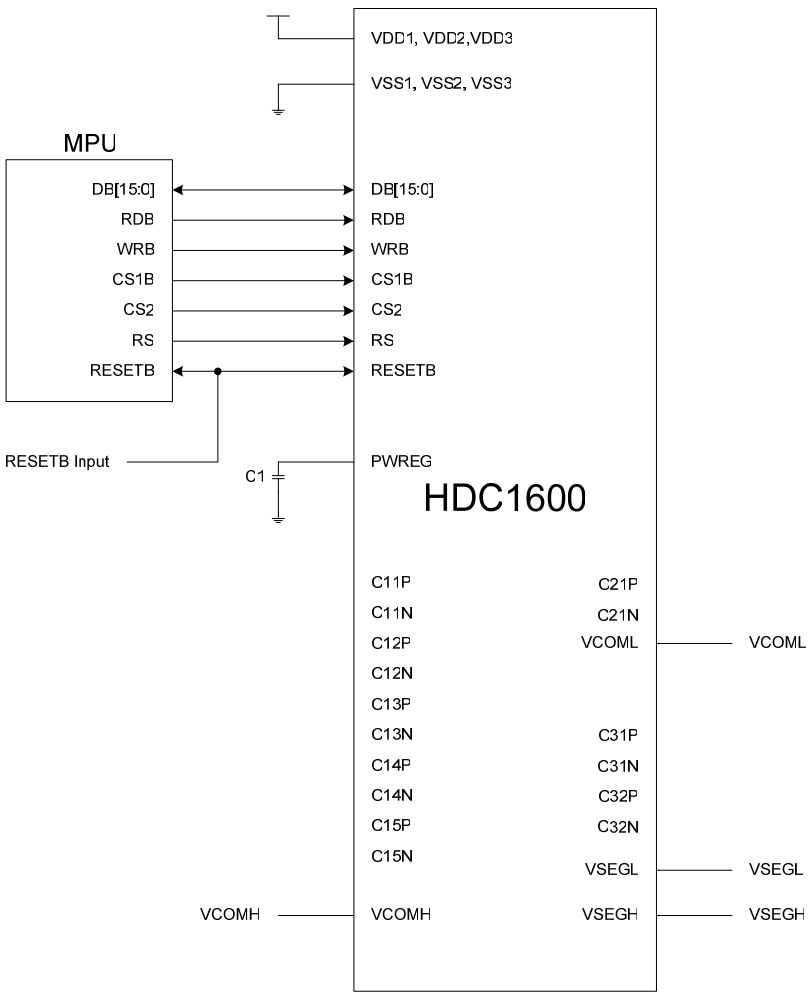
Maximum rating voltage of capacitors

Item	Maximum rating voltage
PWREG to VSS1	4V
C11P to C11N	4V
C12P to C12N	7V
C13P to C13N	10V
C14P to C14N	13V
C15P to C15N	16V
VCOMH to VSS1	18V
C21P to C21N	18V
VCOML to VSS1	18V
C31P to C31N	7V
C32P to C32N	7V
VSEGH to VSS1	4V
VSEGL to VSS1	4V



* Internal power circuit / Internal reference voltage generating circuit are used.
Internal temperature compensation circuit is usable.(2 ~ 6 times boosting programmable)

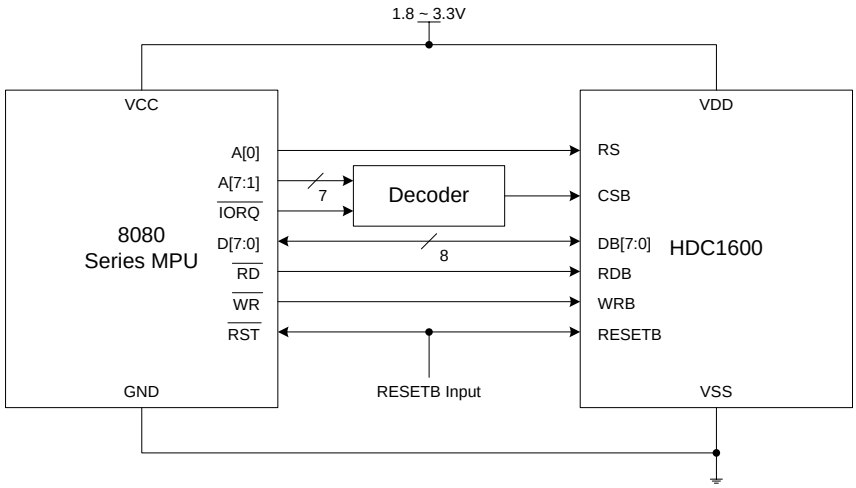
External Power Mode



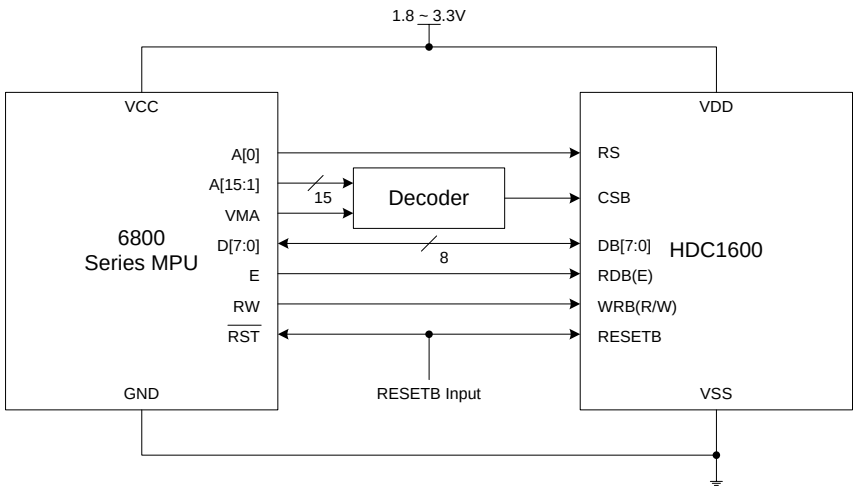
* Internal power circuit is not used (VCOMH, VCOML, VSEGH, VSEGL).

Connection with MPU

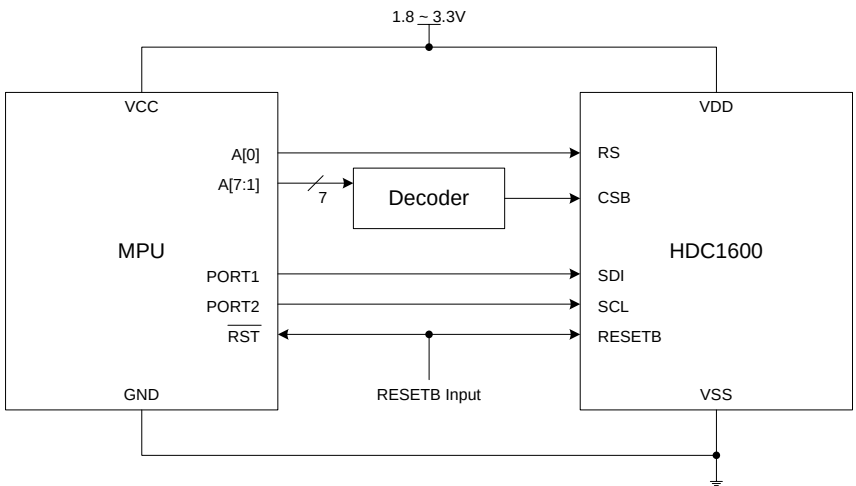
a) 8080-series MPU Interface



b) 6800-series MPU Interface



c) Serial Connection MPU Interface



17. USER TRIM EVOL CALIBRATION MODE

Sequence for setting the modified Electric Volume

Next figure is a Block Diagram of Sequence for Setting the Modified Electronic Volume.

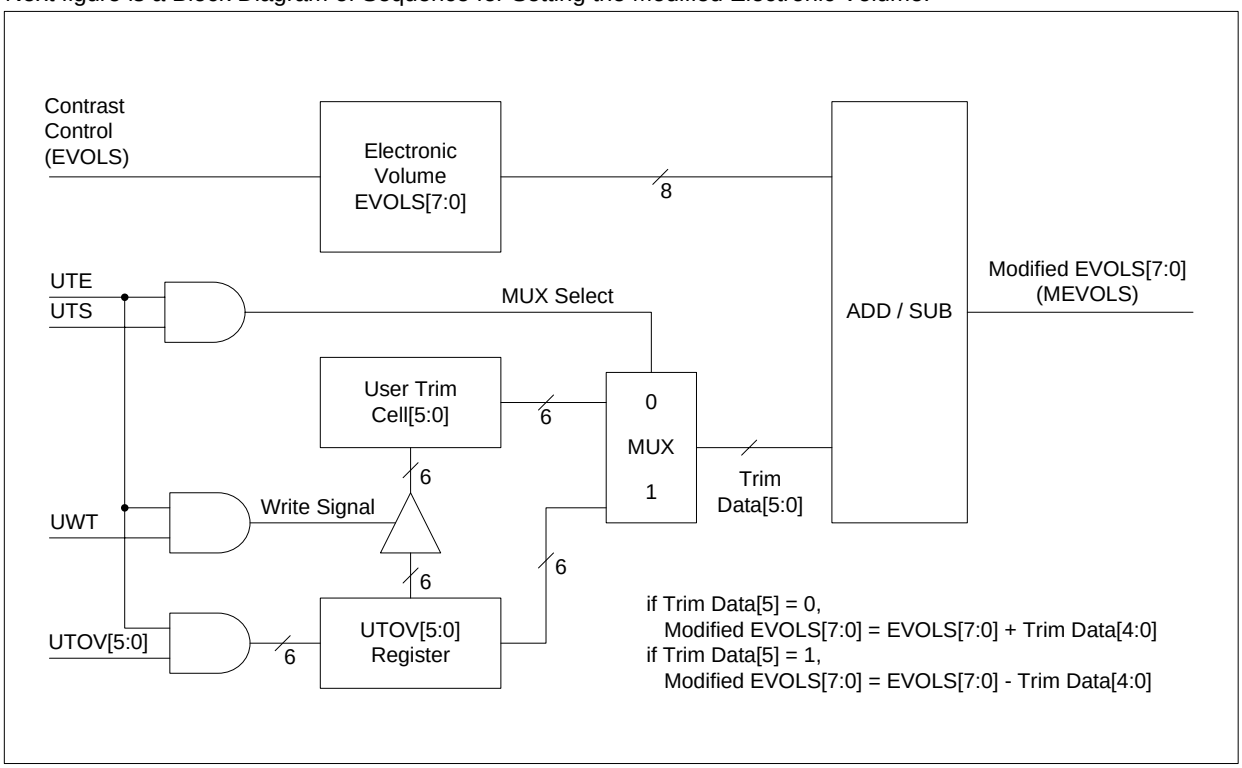


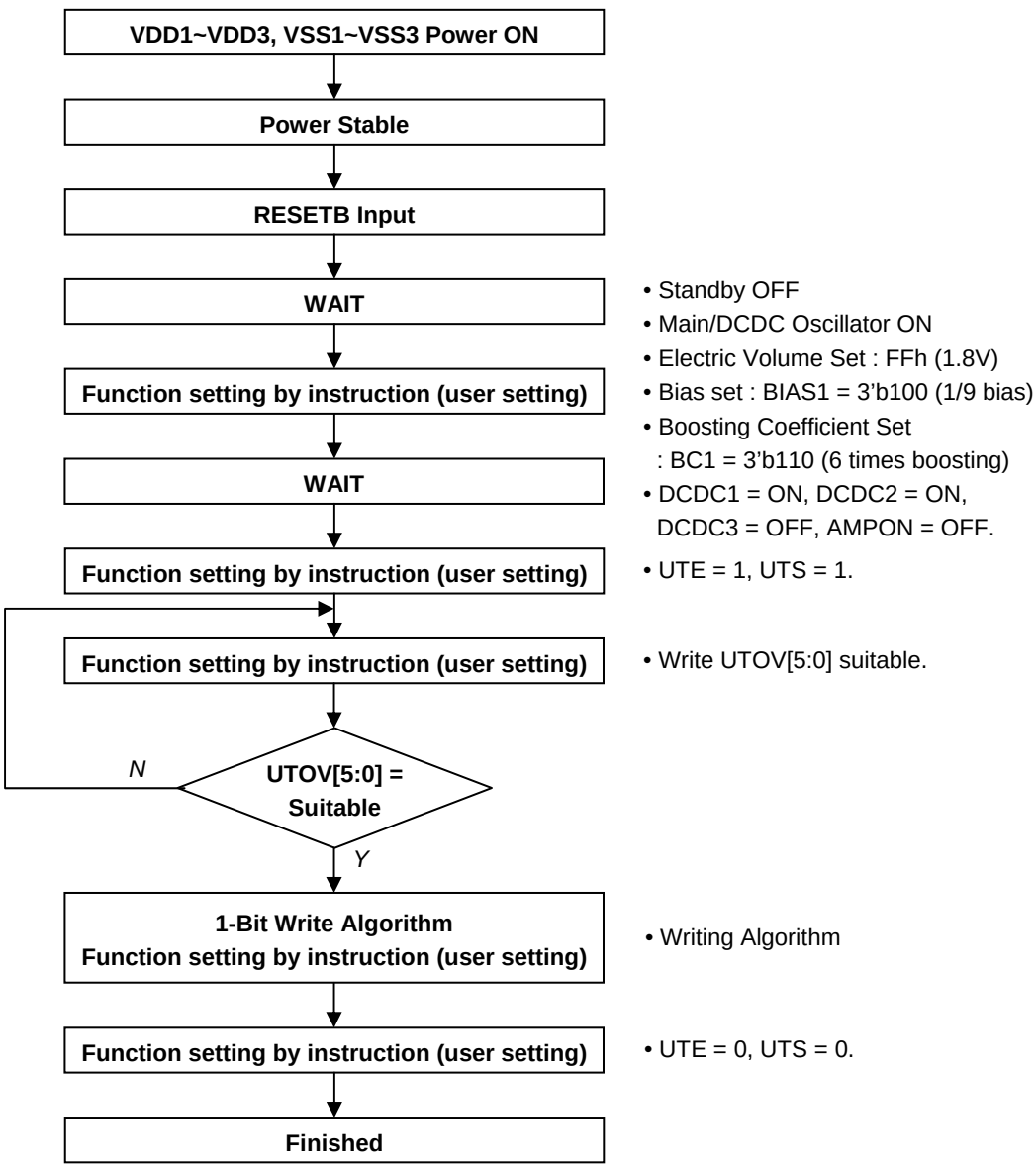
Figure 39. Block Diagram of User Trim Circuit

Initially, User trim cell is not programmed and has 6'b00000 value. When the external reset is applied, User trim mode is OFF (UTE=0, UTS=0, UWT=0, UTOV[5:0]=6'b000000), MUX select is 0. MEVOLS is EVOLS + User Trim Cell. Since MEVOLS is 6'b000000, MEVOLS is EVOLS.

For EVOLS calibration, The instruction "User Trim Mode ON (UTE=1)" and "User Trim/Reg Selection (UTS=1)" is executed, and then MEVOLS is EVOLS ± UTOV and user can adjust MEVOLS value using the instruction "User EVOL Offset Volume Set". When MEVOLS overflows or underflows, MEVOLS will be saturated. Repeat this step until end of the calibration. If MEVOLS calibration is suitable, User trim writing process is executed (UWT=1), and then user trim cell is programmed and user trim cell is programmed with UTOV. Finally, User trim Write disable (UWT=0) and User trim mode OFF (UTE=0) and User trim/reg selection is executed (UTS=0), and then MEVOLS calibration process is finished. As a result, MEVOLS is EVOLS ± User Trim Cell. Accordingly MEVOLS is the EVOLS that has always the offset with user trim cell value.

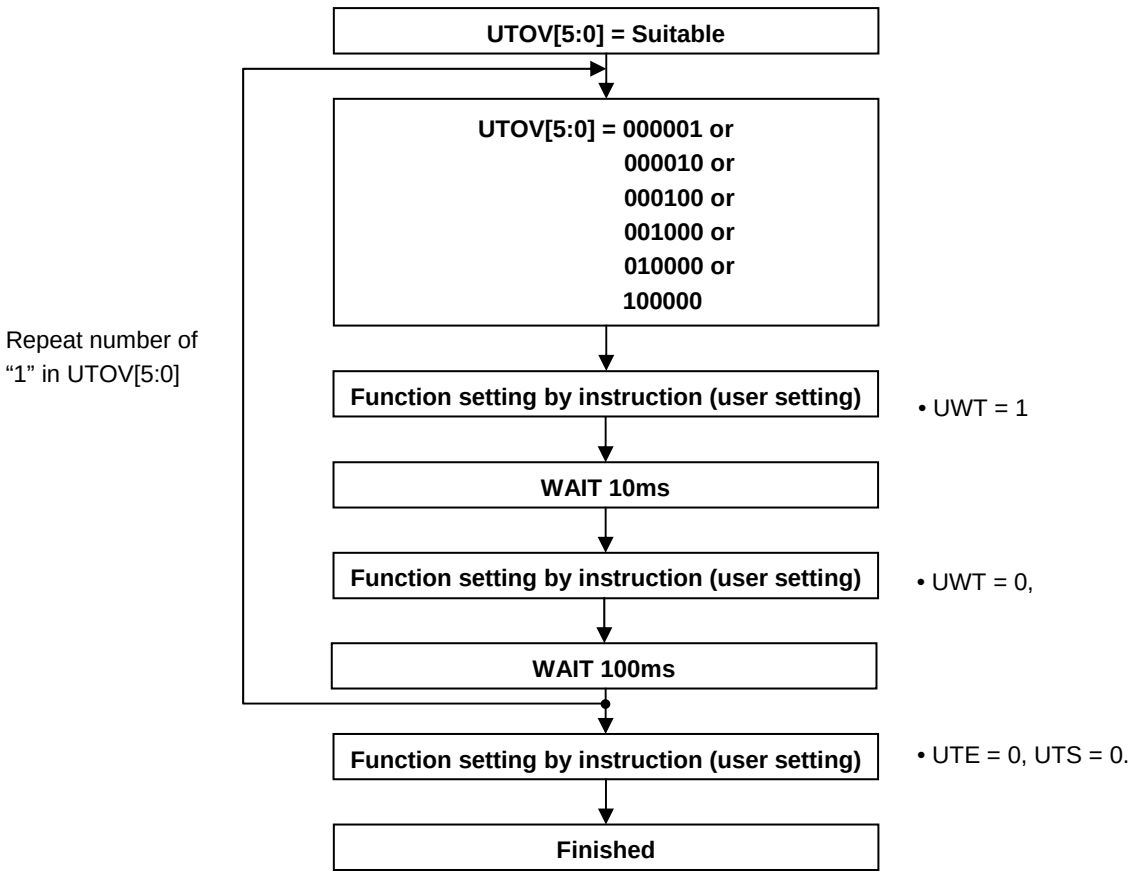
Electric Volume Calibration Flow

User trim cell has been implemented on the HDC1600. The User trim cell stores the offset volume for EVOLS calibration after the device has been assembled and calibrated on a LCD module. The User trim cell block of the HDC1600 consists of 6 bits. and 6 bits are used for EVOLS, EVOLC calibration.



1-Bit Writing Algorithm

1-Bit Writing Algorithm is writing method that repeat writing number of “1” in UTOV[5:0]. UTOV[5:0] step is 3mV.



Example 1)
If Suitable UTOV[5:0] = 000111,
=> 3-Bit Writing is required. because number of “1” is 3.

1) UTOV[5:0] = 000001
2) UWT = 1
3) WAIT 10ms
4) UWT = 0 ; 1-Bit writing finished
5) UTOV[5:0] = 000010
6) UWT = 1
7) WAIT 10ms
8) UWT = 0 ; 2-Bit writing finished
9) UTOV[5:0] = 000100
10) UWT = 1
11) WAIT 10ms
12) UWT = 0 ; 3-Bit writing finished

Example 2)
If Suitable UTOV[5:0] = 111001,
=> 4-Bit Writing is required. because number of “1” is 4.

1) UTOV[5:0] = 000001
2) UWT = 1
3) WAIT 10ms
4) UWT = 0 ; 1-Bit writing finished
5) UTOV[5:0] = 001000
6) UWT = 1
7) WAIT 10ms
8) UWT = 0 ; 2-Bit writing finished
9) UTOV[5:0] = 010000
10) UWT = 1
11) WAIT 10ms
12) UWT = 0 ; 3-Bit writing finished
13 UTOV[5:0] = 100000
14) UWT = 1
15) WAIT 10ms
16) UWT = 0 ; 4-Bit writing finished

REVISION HISTORY

HDC1600 Specification Revision History			
Version	**Content**	**Author**	**Date**
0.1	Original	J.J. Park	May.01.2005
0.2	1.Correct PAD COORDINATES. 2.Add schottky diode in SYSTEM APPLICATION DIAGRAM.	J.J. Park	Aug.01.2005
0.3	1.Modified DCOSC Frequency. 2.Correct misprinted Figure 30. Relation of EVOLS, EVOLC, User Trim. 3.Add standby mode flag initial status. 4.Modified Table9,10 Red / Green / Blue Palette Gradation Table. 5.Modified EVOLS 1 Step 6mV => 3mV. 6.Add 1-Bit Writing Algorithm in user trim. 7.Modified X-address => Y-address, Y-address => X-address in display memory address. 8.Correct bumped PAD height : 15um => 17um. 9.Modified dc/ac characteristics. 10.Add MPE ON/OFF sequence. 11.Add VCOML ITO resistor limit (30Ω and below).	J.J. Park	Sep.01.2005
0.4	1.Remove VCOML ITO resistor limit and schottky diode in SYSTEM APPLICATION DIAGRAM. 2.Modified dc/ac characteristics. 3.Correct bump PAD size.	J.J. Park	Oct.27.2005
0.5	1.Correct Status Read REV=>SDP0. 2.Correct LCD driver output RON resistance.	J.J. Park	Nov.18.2005
0.6	1.Modified 1-Bit Writing Algorithm in user trim. 2.Modified EVOLS1,2 range(0.935V~1.7V => 1.035V~1.8V). 3.Correct maximum rating voltage C31P,C31N,C32P,C32N (18.0V =>7.0V)	J.J. Park	Dec.22.2005